EECS:290C RFIC Architectures & Circuits for Modern Wireless Communication Systems

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office hours: Tue, Thu 9:30am-10:30am (shortly after class)

- **Class objectives**
- **Grading**
- **Course outline**

Class objectives:

● Hands on experience in the art of system architecture and circuit design for RF systems, with great emphasis on practical considerations.

● Develop design methodologies and techniques for optimizing RF circuits

● Create proper understanding of basic tradeoffs

● Create proper feeling of what a given technology can offer, (CMOS, bipolar, BiCMOS)

Prerequisite*: Good circuit fundamentals.*
having taken EE142 and/or 242 is a plus but is not a must

Grading:

- 60% homework

Please collaborate! In the real world you will be part of a team and need to

learn how to work in a team. However, do not copy each other. Use discussions to enrich your understanding of the subject but then you need to come up with your own design and solution to submit and defend. This is how it is in the real world!

Will be using **T28 CMOS process** for homework.

- 40% project:

The project will be to design an RF or baseband block to fit a specific RF standard. A group of students might opt to design an entire RF receiver (from antenna to baseband including LO generation). We will settle on a specific technology for the project (CMOS). The details and formality of the project will be finalized later. The project starts right after the midterm exams.

Lecture notes:

- can be downloaded from the bCourse website:

https://bcourses.berkeley.edu/courses/1477110

- Please print lecture prior to coming to class to take your own notes. If you want to stay “green”, download an electronic copy on your tablet and take electronic notes

- bCourse will be used to communicate with students for blast emails.

CAD tools:

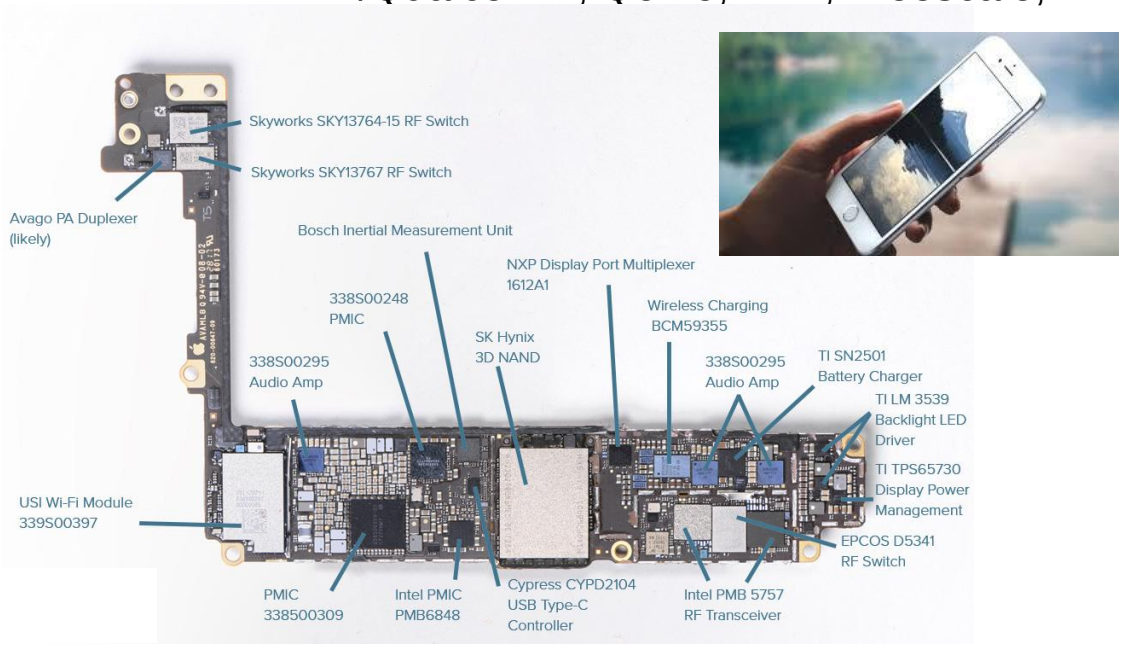
- will be using SpectreRF for circuit simulation
- need a volunteer to help me with CAD related issues (someone to help fix CAD issues in UCB CAD environment or knows how to get help). This role is not needed if you all know how to do so

Why this class is good for you?

- wireless transceivers are everywhere!

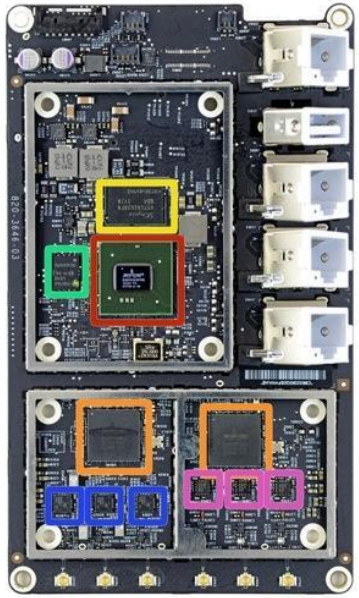
1. Cellular: 2G(GSM/GPRS), 3G(WCDMA/UMTS), 4G(LTE), 5G (sub-6GHz and mmWave)

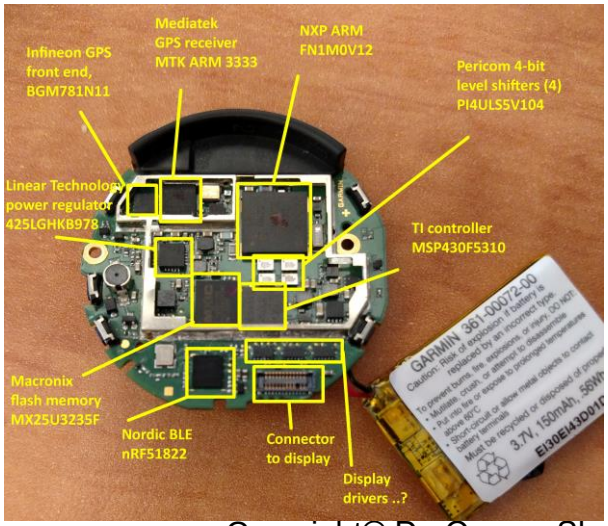
- Cell-phone transceiver (client): Qualcomm, MediaTek, Intel/Infeneon, Samsung, Spreadtrum, Huawei
- Base-station transceiver (AP): NXP, Ericson, Huawei, ADI
- Font-end modules: Skyworks, Broadcom/Avago, Murata, TDK/Qualcomm, Qorvo, NXP, Freescale, ADI



2. Connectivity:

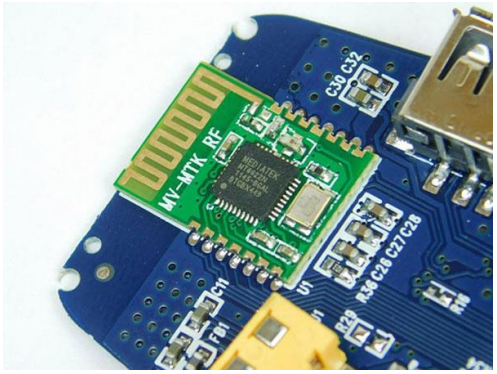
- WiFi transceiver: Broadcom, MediaTek, Intel, Qualcomm/Atheros, RealTek, Marvell, Samsung, Apple
- GPS/GNSS: Broadcom, MediaTek, SiRF, Qualcomm/CSR, Samsung
- Bluetooth: Broadcom, MediaTek, Qualcomm/CSR, Samsung, Apple, Marvell
- IoT: SiLab, Nordic, MediaTek/Airoha, Cypress, tons of startups
- mmWave (60GHz): AMD/Netero, Apple





3. Broadcast:

- SATCOM: IDT
- FM: Broadcom, MediaTek, Qualcomm/atheros, SiLab, Broadcom
- TV tuners: SiLab, MaxLinear, Sony, Mstar/MediaTek,
- Set-top Box: Broadcom, MaxLinear, Maxim Integrated



Course outline:

Part I: System Architecture, an overview

- most popular Rx radio architectures
  - Superhetrodyne
  - Dual conversion image rejection architecture
  - Direct-Conversion
  - Low-IF
  - Dual-Conversion Double-Quad
- Broadband Rx radio architectures
  - Up-down conversion
  - Harmonic-rejection direct conversion
  - Spectrum capture
- system requirements and impact on circuit design, current consumption and chip area
  - Sensitivity
  - Linearity
  - Gain, Dynamic-range
  - Selectivity
  - EVM

Course outline:

Part I: System Architecture, an overview .. 'Cont

- o most popular Tx radio architectures
  - DCT, Direct Cartesian Transmitter
  - Polar
  - Outphasing
  - Digital transmitter
- o system requirements and impact on circuit design, current consumption and chip area
  - EVM
  - Emission mask
  - FCC emission
  - CIM3
  - ACLR
  - Dynamic-range, TPC
  - LO feed through
- o system calculation using spreadsheet and radio analysis

Part II: RF Receiver Front-End Design

- LNA design
  - Optimum vs. minimum NF biasing
  - Simultaneous NF and power match
  - Design for linearity vs. design for low power
  - BJT LNA vs. CMOS
  - A practical example of a WiFi LNA design
- Mixer design
  - SSB vs. DSB NF definition
  - Single-balanced vs. double-balanced mixers
  - Most popular mixer circuit topologies
    - Gilbert-cell mixer
    - FET passive mixer
    - Current-mode mixer
    - Sub-harmonic mixer
  - Noise and linearity analysis
  - A practical example of a mixer design

Part III: Receiver Baseband Design

- Baseband filters
  - Introduction to filters
    - Why filters are needed in an RF receiver
    - Filter functions & specifications
  - How to specify a filter for a certain system
  - Integrated filter Architectures
    - Ladder, Cascade
  - Integrated filter topologies
    - Opamp-RC, Gm-C, Current-mode, log-domain
  - Filter tuning
  - Complex filters

- Variable-Gain Amplifier, VGA, design
  - Why a VGA is needed in an RF system
  - VGA specifications
  - DC-offset and how to deal with it
  - Digital/analog-gain control (linear dB/code or /V)
- A practical baseband example

Part IV: Voltage-Controlled Oscillator Design

- VCO specifications and their impact on radio performance
  - Phase noise
  - Tune range and Kvco
  - Load pulling
  - Supply pushing
  - Spectral purity
  - design issues with LC integrated VCO
    - On-chip varactors, inductors and capacitors
    - How to chose the LC tank components
    - VCO biasing
    - VCO loop-gain
    - VCO tank design and temperature compensation
    - VCO buffers and on-chip supply regulator design
  - Phase-noise analysis
  - Wide-band VCO design

- A practical example

Part V: LO generation and LO distribution schemes

- The issue of VCO/LO pulling
  - theory
  - Spur analysis
- Integer LO generation scheme
- None-integer LO generation scheme
- LO buffer design
- practical considerations

Part VI: Transmit basic building blocks

- Up-converter design
  - Active Gilbert-cell up-converter
  - Passive up-converter
    - The issue of asymmetry in passive up-converters
- RF VGA/PGA design
  - Current-steering
  - slicing
- practical considerations

Part VII: Power Amplifier Design

- Single-ended vs differential
- Load-pull
- Output balun/OMN
- PA class (A, AB, B, C, D) and efficiency
- Memory effects
- PA efficiency enhancing techniques:
  - Doherty, outphasing and digital PAs
  - Envelop tracking

Part VIII: On-chip T/R Switch Design

- Design challenges of on-chip T/R switch
  - Breakdown, Isolation and Loss
  - ESD
- practical T/R design topologies
  - MOS-based T/R switch
  - Passive LC T/R switch

Part IX: mmWave Phased Array

- Basic concepts of a phased-array
- Tx Pout and Rx SNR calculation
- Essential building blocks of a phased array
- Beam shaping techniques
- mmWave circuits:
  - Phase shifter
  - Gain equalizer
  - LNA
  - PA
  - VGA
  - T/R switch
  - Up/dn converters

- **Part X: PLL Design**
  - PLL specifications and its impact on RF system
    - Divide range
    - Comparison frequency
    - Channel spacing
    - Settling time
    - Capture range
    - Integrated phase error
    - Stability
    - Spectral purity
  - Integer-N PLL architecture and loop analysis
    - 3/2 prescalar design and analysis
    - CMOS digital divider design
    - PFD design and analysis
    - Charge-pump design
    - Design of loop filter

- Fractional-N PLL architecture & design
  - Conventional Frac-N architecture
  - Σ-Δ Frac-N architecture
  - Design of Σ-Δ modulator
  - Verification of Frac-N PLL using Matlab
  - Design of loop filter

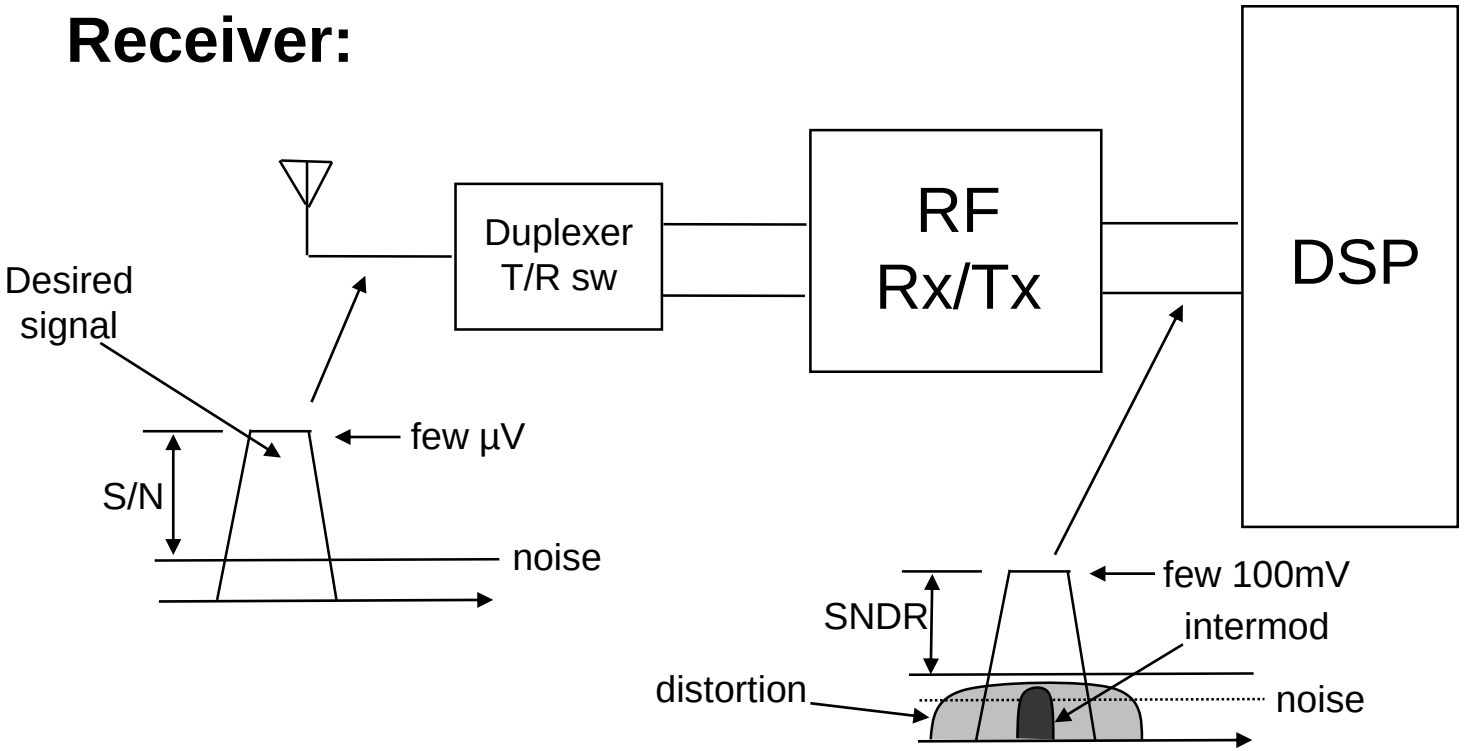
- All-digital PLL
  - TDC
  - DCO
  - Digital loop filter

Introduction to Radio Architecture

- **Radio design, the big picture**
- **Important high-level specs of a radio transceiver**
  - **Rx**
  - **Tx**
  - **LO**

Radio design- the big picture:

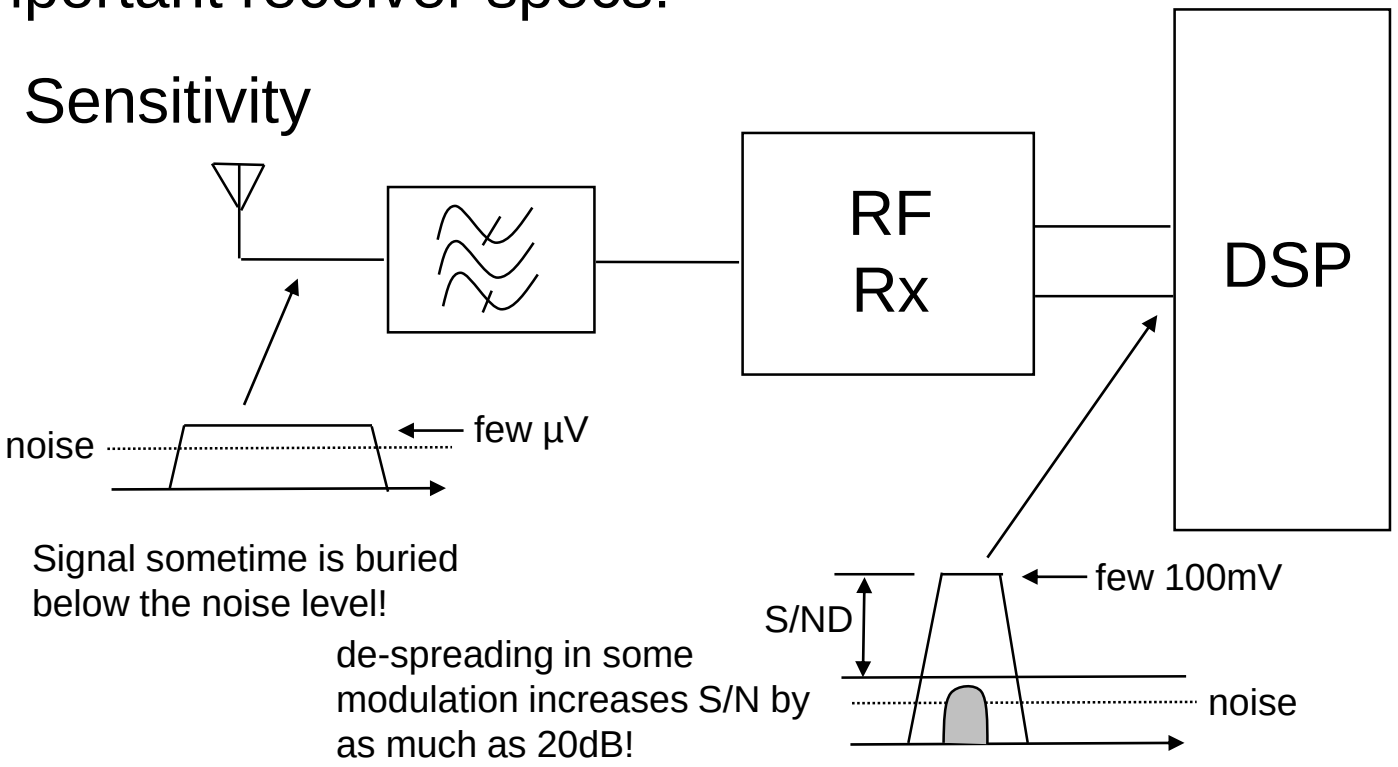
Receiver:



Receiver output SNDR not to be lower that the required level for min BER under ALL conditions for a given standard/modulation

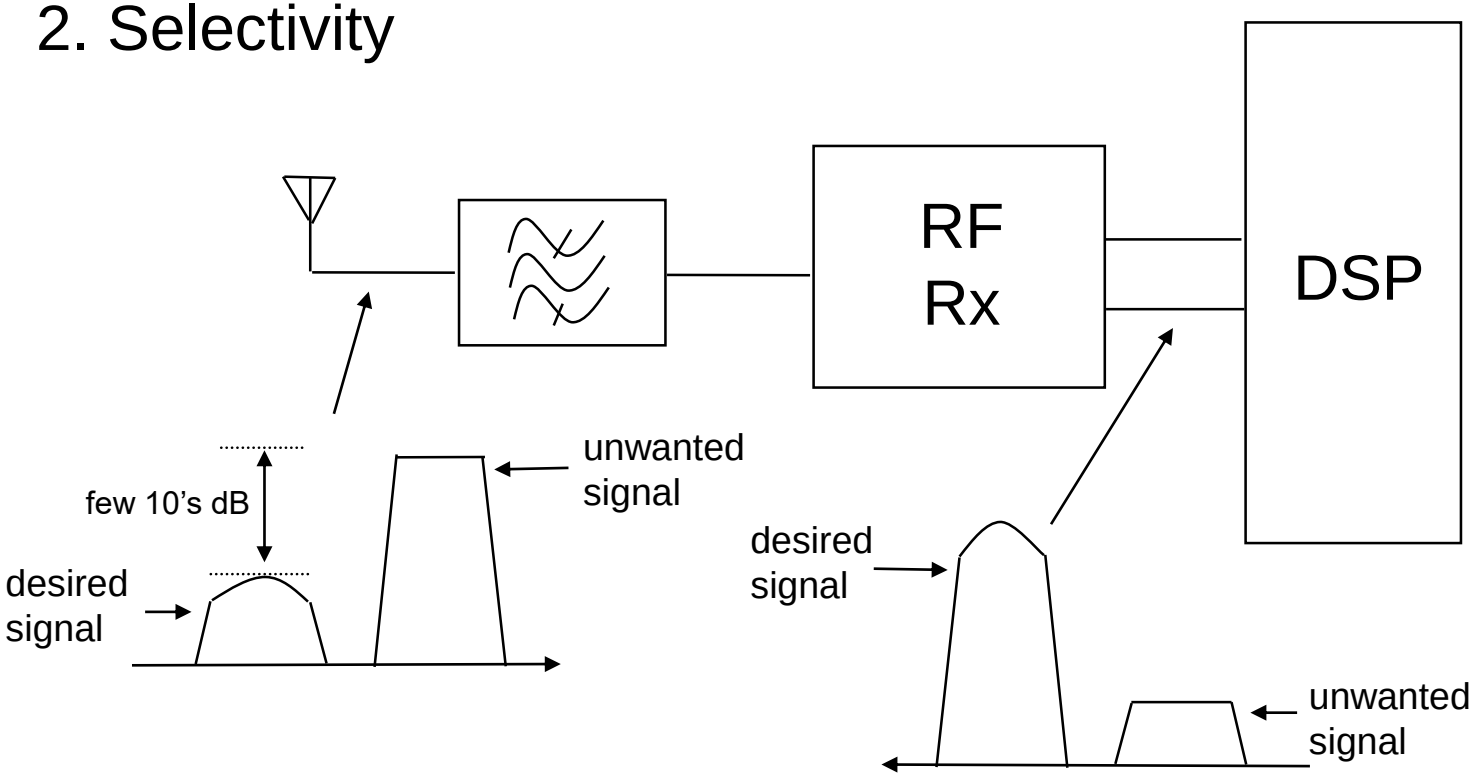
Important receiver specs:

1. Sensitivity



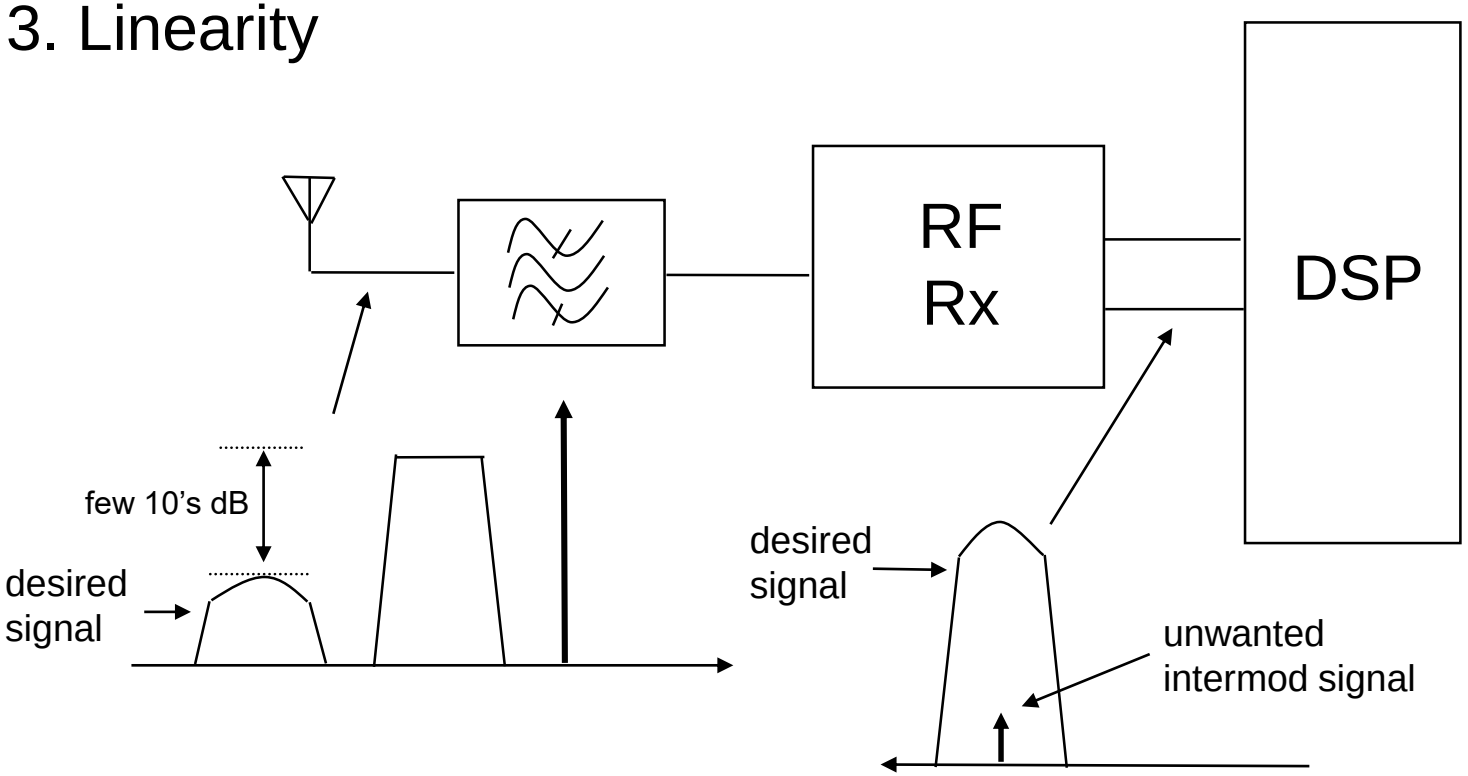
Sensitivity is the lowest input signal level (in dBm) detectable by the receiver while still meeting the min acceptable BER at the DSP detector

2. Selectivity



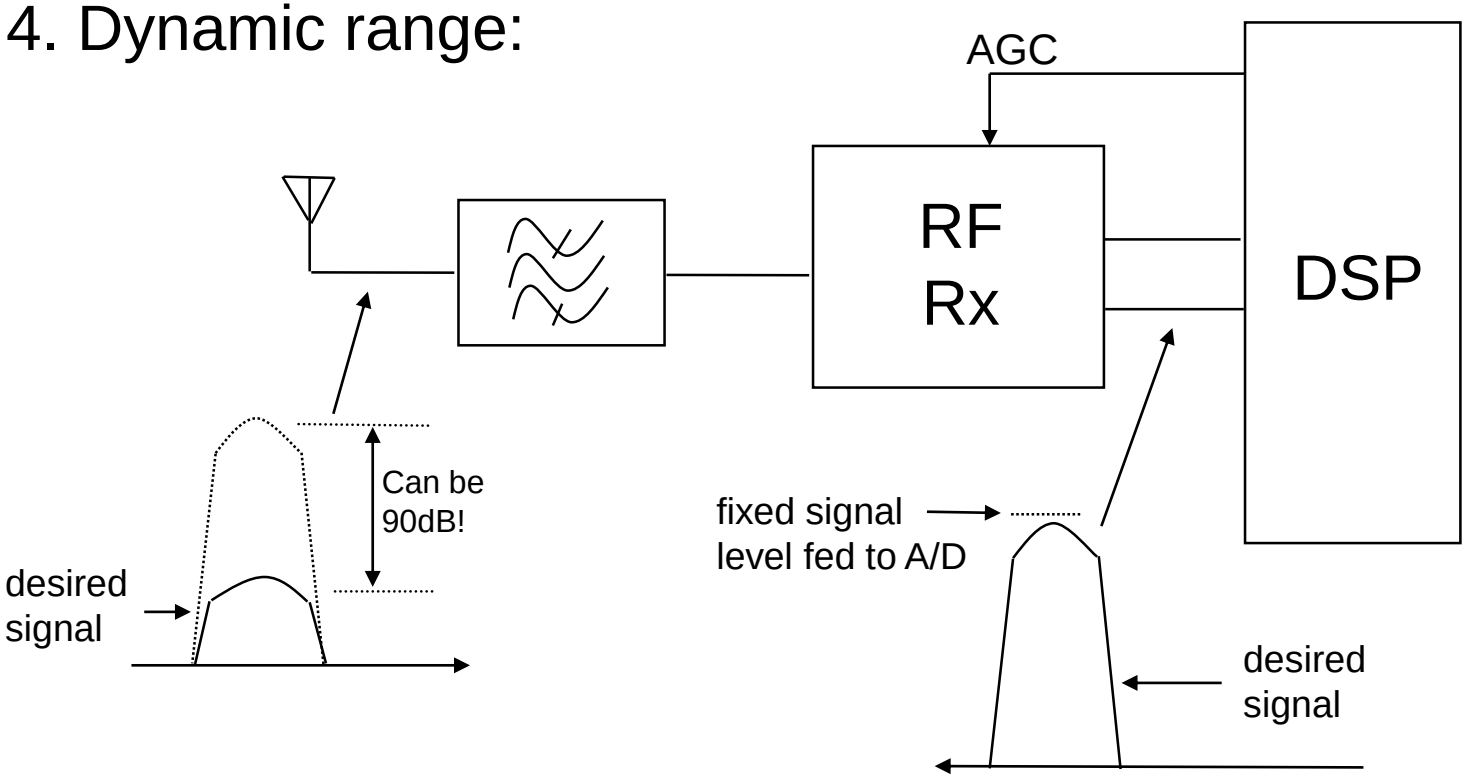
Selectivity is the level ratio of desired signal to all other "unwanted" interferers in dB (integrated over the signal bandwidth). The interferer is sometimes as high as 60dB above the desired signal!

3. Linearity



Rx Linearity is defined in terms of 3rd and 2nd order distortion/intermod levels at the receiver output calculated from the overall acceptable noise+distortion at the detector

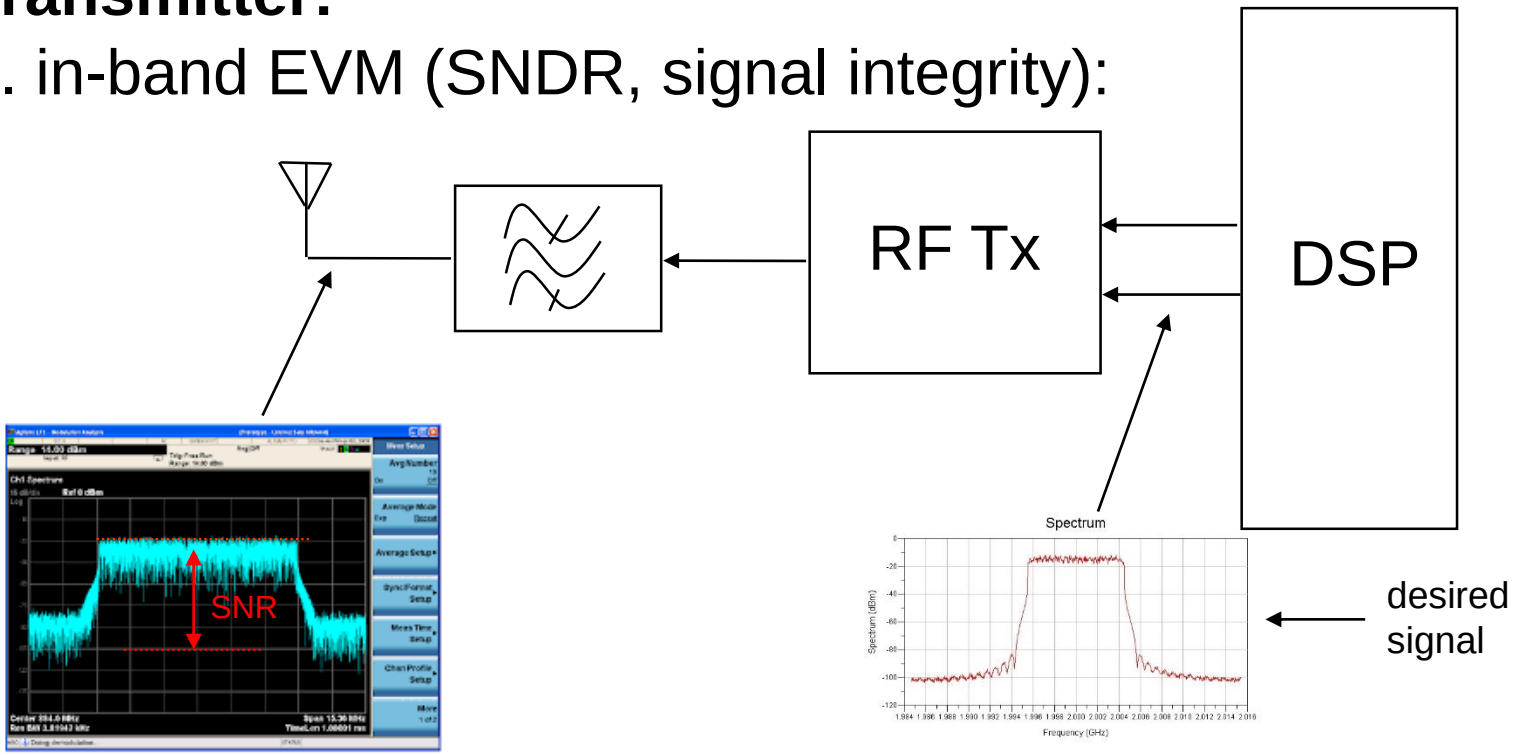
4. Dynamic range:



Receiver must sustain a fixed signal level to DSP A/D despite the variation of the desired signal level at the antenna by as much as 90dB (dynamic range). The level is set by the A/D dynamic range

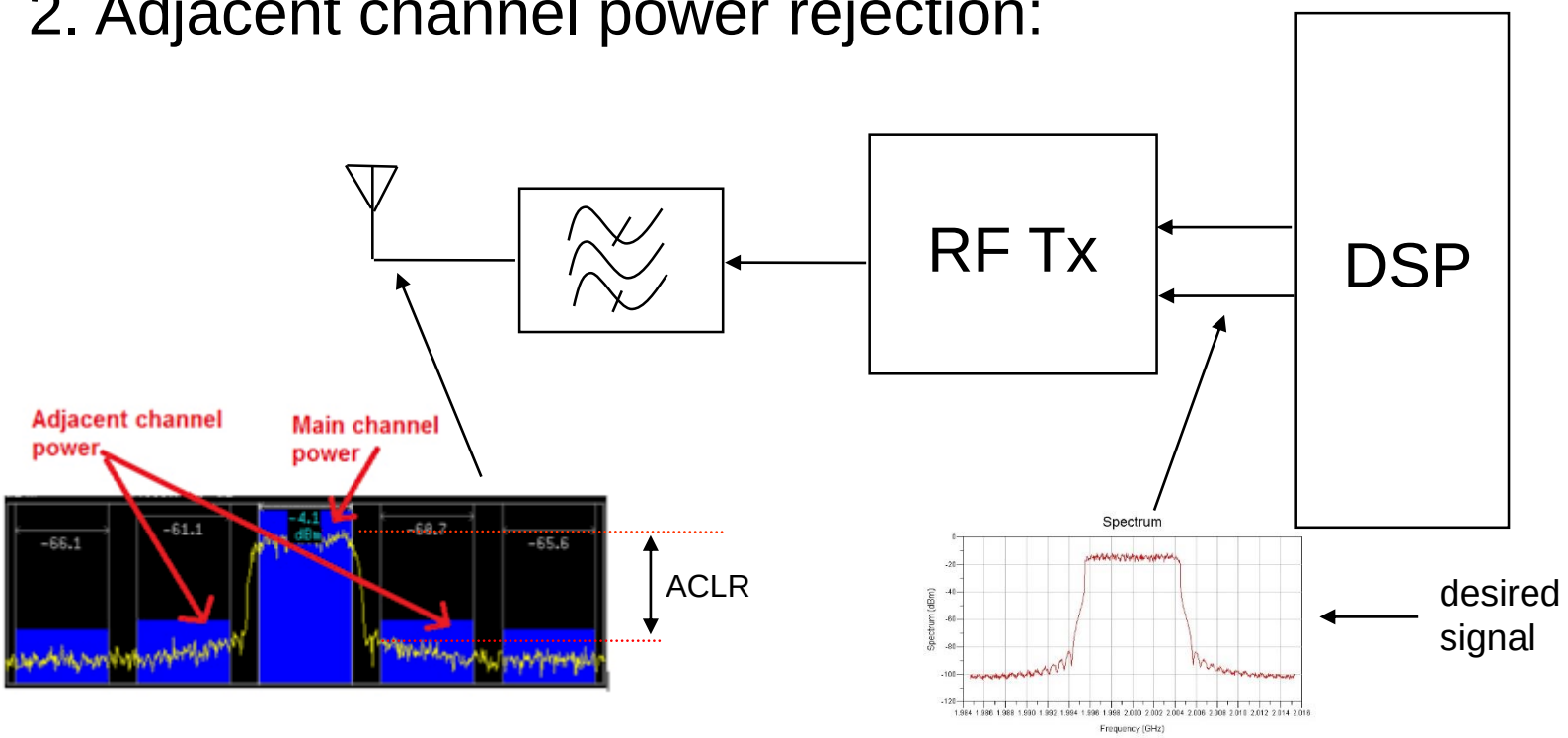
Transmitter:

1. in-band EVM (SNDR, signal integrity):



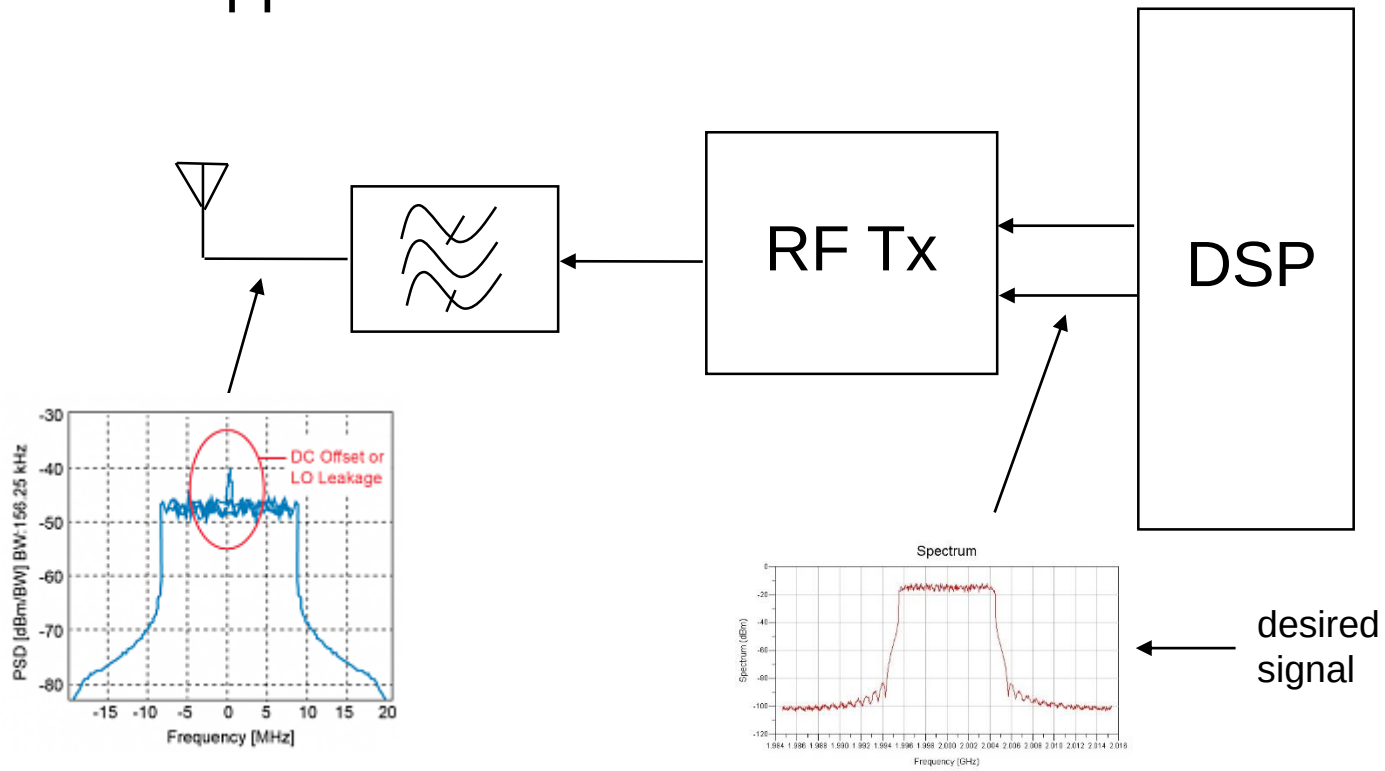
Due to finite transmitter linearity ad circuit noise, the SNR of Tx signal is degraded. It is essential the Tx keeps the in-band signal SNDR (~EVM) at or better what is specified by the standard (WiFi, 3GPP, etc.) so other receivers can decode it

2. Adjacent channel power rejection:



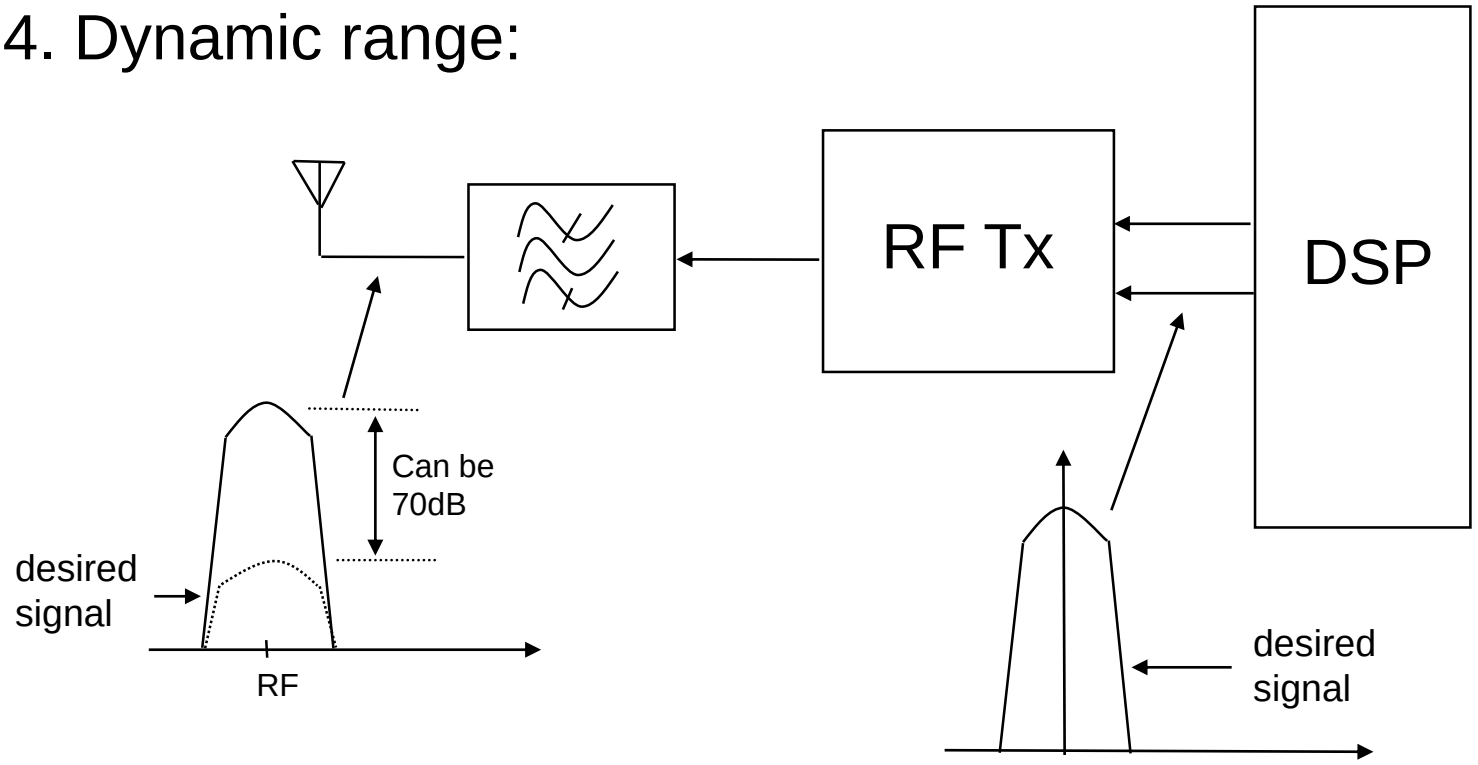
Due to finite transmitter linearity and noise, some of the unwanted transmitted power falls on the adjacent channel frequency band. The ratio between the transmitted power of the desired band over that of the adjacent cannel is the Adjacent Channel Level Rejection (ACLR)

3. Carrier suppression:



standard regulates a certain carrier suppression requirement. The ratio between signal level and carrier in dB (over specific RBW) is the carrier suppression

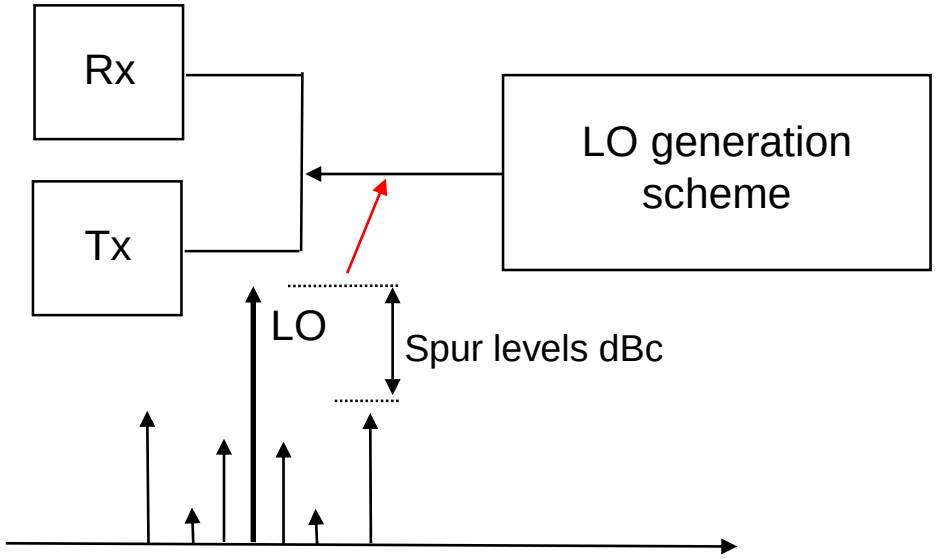
4. Dynamic range:



Transmitter must adjust its output power depending on how close the system is to a base station. The range of the adjusted power is the Tx dynamic range.

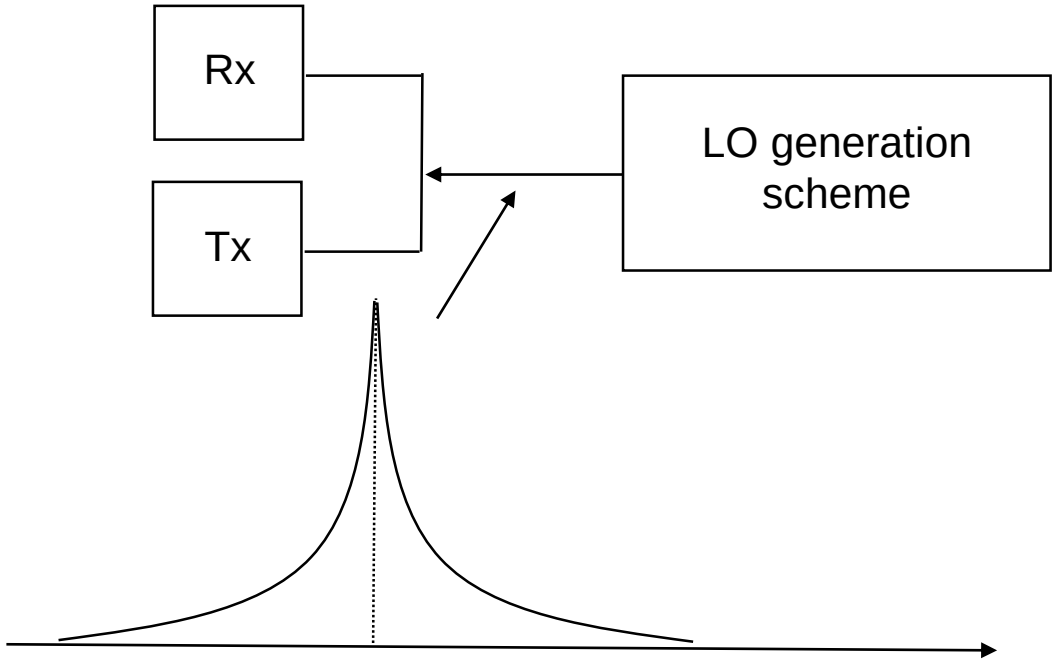
LO generation:

1. Spectral purity:



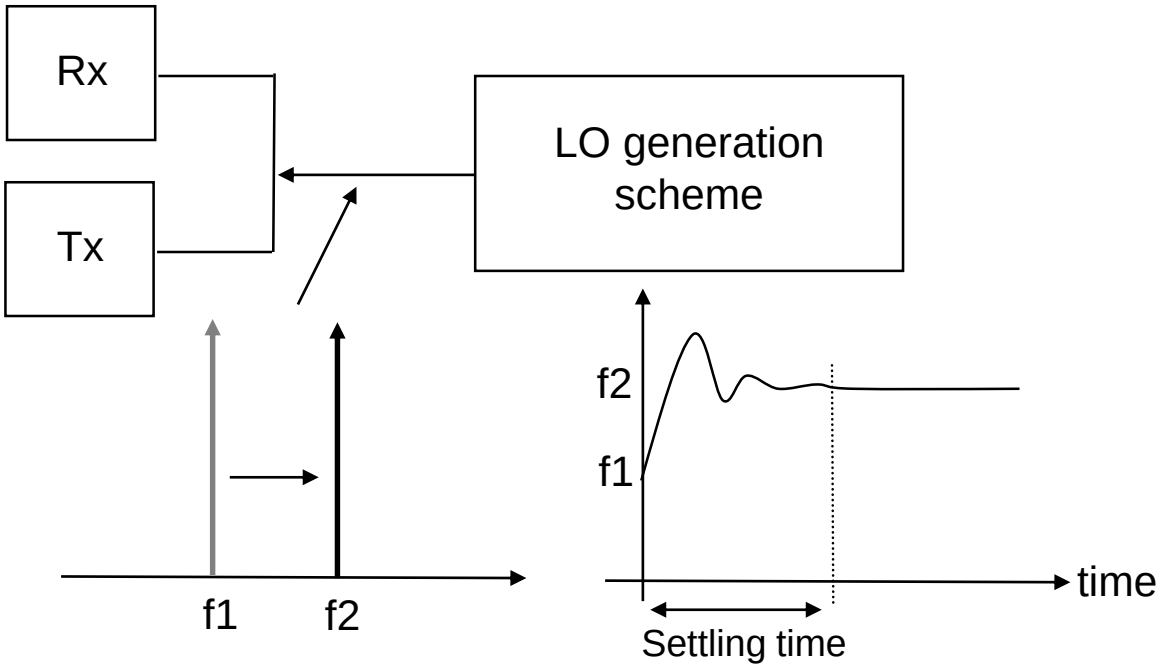
The spectral purity of the LO generation scheme is defined as how many dB down are the worst case spurs relative to the desired LO signal

2. Spectral noise density:



The integrated phase noise under the LO skirt translated into phase jitter in the time domain. The LO phase noise is important for both S/N and EVM.

3. Spectral settling time:



The LO generation is required to settle within few kHz within specified number of µs so as not to lose any Rx packet or corrupt the Tx spectral mask.

In this class, we will go over all various blocks comprising receivers, transmitters and LO generation and dive deep into their design, specifications, tradeoff and optimization with clear understanding of radio architectures and system specifications.