EECS 290C: Advanced circuit design for wireless
Homework # 1
Due Thu 02/07

Q1.
a) For the architecture of figure 1, due to circuit mismatch and value tolerance, the values of the phase shifter might not be exactly 90. Assume the 90° LO path phase shifter is off by 1 degree. Assuming everything else is perfect, how much is the achievable image rejection in dB?

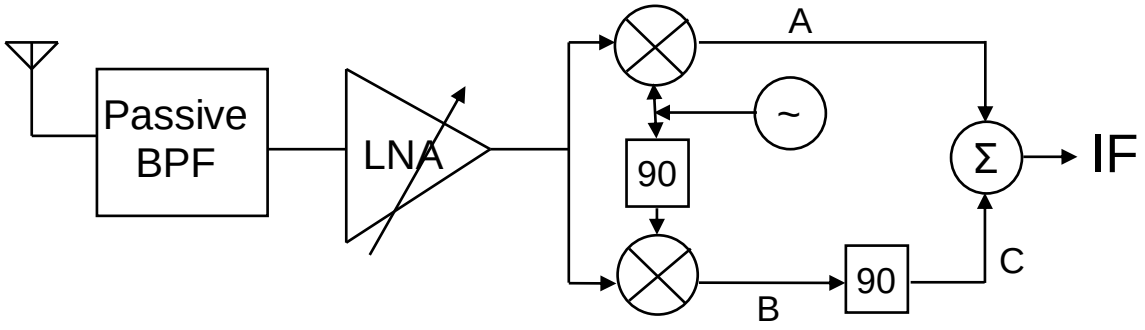

Figure 1

b) if the down conversion mixers have a gain mismatch of 1dB, assuming everything else is perfect, how much is the achievable image rejection in dB?

c) Draw the constant image rejection contours vs. gain and LO phase mismatch. You can use any tool you like (SPICE, Matlab, ADS, C++, etc.).

Q2.
For the double-conversion double-quad architecture, show that the phase mismatch of the overall radio is the product of the phase imbalance of both down conversion stages.

Q3.
a) Construct a spreadsheet to calculate the gain, IIP3, and NF for the direct conversion architecture in figure 2, referred to the antenna port:

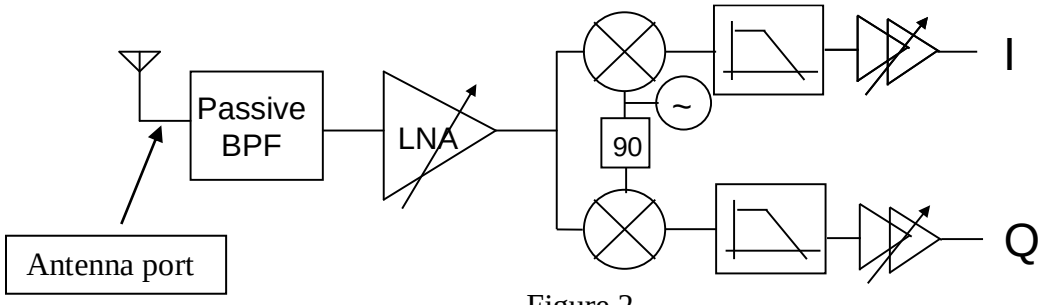

Figure 2

Assume input impedance of LNA is 50Ω, LNA-mixer interface has a 400-ohm impedance on chip, the mixer load is 900Ω differential, filter input is high-Z, and the VGA drives a >10kΩ//5pF differential load. Also assume the external SAW BPF loss is 1dB.

b) Plug in *feasible* gain, IP3 and NF values for different blocks to create a receiver with NF <4dB, IIP3>-14 and >95dB of voltage gain.

Hint: a skeleton spreadsheet will be provided on the class website as a starting point.

Submit your spreadsheet to osama.shanaa@berkeley.edu