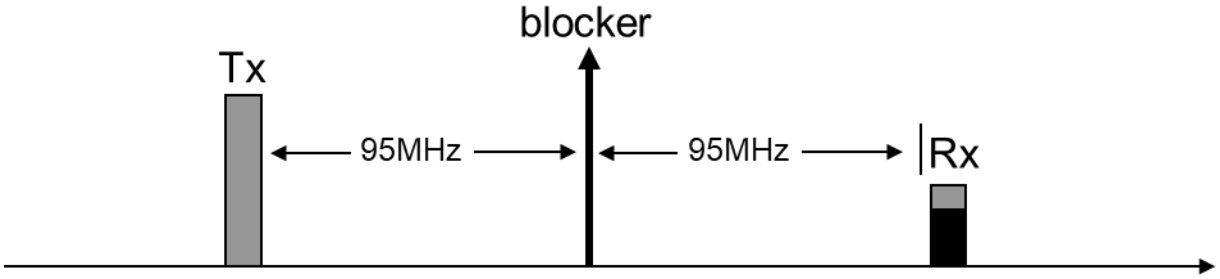
EECS 290C: Advanced circuit design for wireless
Homework #2

Q1. This question is intended to give you the relationship between sensitivity and both signal bandwidth and required SNR:

A 5.5GHz RF system supports two different types of modulations; MCS1 and MCS8. It also supports two different signal bandwidth (RF bandwidth); 20MHz and 160MHz.

For the same receiver that has a total noise figure (NF) of 4dB at room temperature, calculate the receiver sensitivity in dBm (also at room temperature) for both modulations with the two possible signal bandwidth. Assume the demodulator required SNR is 4dB and 25dB, for MCS1 and MCS8, respectively.

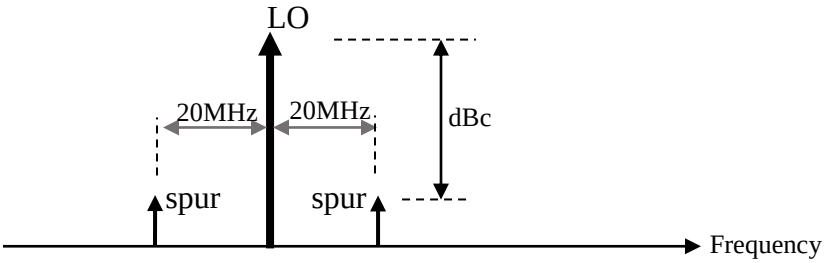
Q2. For the WCDMA receiver IM3 due to intermodulation between Tx leakage power and blocker in Band I (B1) shown below.



The Tx leakage is -27dBm after diplexer. The B1 blocker level is -15dBm at antenna. In class, we calculated the receiver IIP3 requirement due to this arrangement for a diplexer rejection of 30dB at B1 (result came as -7.9dBm without margin). Let us assume you found another diplexer that provides 31dB rejection to blocker at B1 (1dB better than the one we used in class), how much the receiver IIP3 can then be relaxed by? (Assume Tx leakage remains the same as before with this new diplexer)

Q3. This question is intended to calculate LO spur level requirement:

A PLL uses a 20MHz reference crystal oscillator that results in a reference spur +/- 20MHz away from the LO used for a WCDMA receiver as shown below:



With the adjacent channel n+4 (or 20MHz away from desired signal) level of -40dBm, calculate the relative spur level in dBc (relative to the main LO) so that the folded n+4 signal in-band due to the PLL spur has a negligible impact on the receiver sensitivity of -117dBm.

Q4. This question is intended to refresh your RF matching knowledge to be ready for the following homework problems.

a. Let us assume an RF receiver block has an input impedance (Zin) of 10-ohms (real, no imaginary) at 2.5GHz. Design an L-match network to power match this impedance to a 50-ohm source. There are two possible ways to do an L-match; a series inductor followed by a shunt capacitor or a series capacitor followed by a shunt inductor. You need to design both if feasible. Assume the matching components are ideal (infinite Q). Plot S11 using Spectre. Also plot the matching network voltage gain (Vout @ the input ports of the DUT vs Vin @ the RF port terminal).

b. Replace the ideal inductors in your matching network in (a) with finite Q inductors (Q=10 to mimic on-chip spiral inductors, assume finite Q is mainly due to series resistance of inductor winding).With the aid of Spectre, re-simulate your matching network in (a). Feel free to "tweak" the components of your matching network to get a good S11 (<-12dB). Re-plot S11 and matching network voltage gain.

c. If the RF block impedance has additional capacitive reactive component of –j50 (so total input impedance is 10-j50 ohms), re-design your matching network to match this to a 50-ohm source. See if both L-match ways are still possible. Use ideal components first. Report S11 and matching network voltage gain. Repeat this step with inductor Q of 10.