EECS 290C: Advanced circuit design for wireless
Homework #2 **Solution**

Q1. This question is intended to give you the relationship between sensitivity and both signal bandwidth and required SNR:

A 5.5GHz RF system supports two different types of modulations; MCS1 and MCS8. It also supports two different signal bandwidth (RF bandwidth); 20MHz and 160MHz.

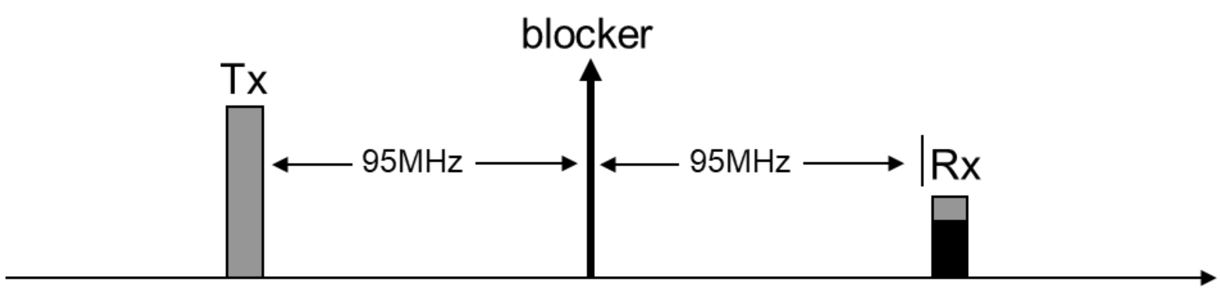
For the same receiver that has a total noise figure (NF) of 4dB at room temperature, calculate the receiver sensitivity in dBm (also at room temperature) for both modulations with the two possible signal bandwidth. Assume the demodulator required SNR is 4dB and 25dB, for MCS1 and MCS8, respectively

Answer:
MCS1:
Noise power (dBm) = -174dBm/Hz +10logBW + NF = -97dBm (for 20MHz BW) and -88dBm (for 160MHz BW)

Sensitivity (dBm) = noise power (dBm) + SNR (dB)
Sensitivity (20MHz) = -97dBm + 4dB = **-93dBm**
Sensitivity (160MHz) = -88dBm + 4dB = **-84dBm**

Repeat for **MCS8**:
Sensitivity (20MHz) = -97dBm + 25dB = **-72dBm**
Sensitivity (160MHz) = -88dBm + 25dB = **-63dBm**

Q2. For the WCDMA receiver IM3 due to intermodulation between Tx leakage power and blocker in Band I (B1) shown below.



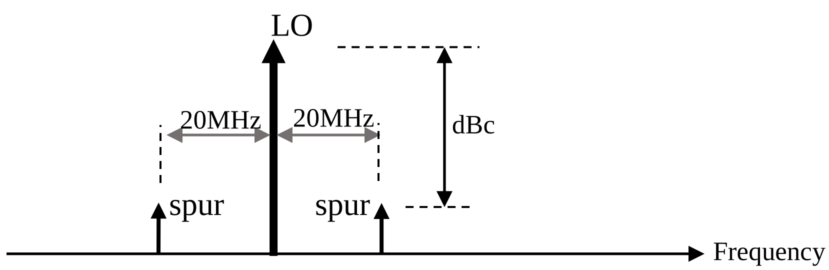
The Tx leakage is -27dBm after duplexer. The B1 blocker level is -15dBm at antenna. In class, we calculated the receiver IIP3 requirement due to this arrangement for a diplexer rejection of 30dB at B1 (result came as -7.9dBm without margin). Let us assume you found another diplexer that provides 31dB rejection to blocker at B1 (1dB better than the one we used in class), how much the receiver IIP3 can then be relaxed by? (Assume Tx leakage remains the same as before with this new duplexer)

Answer:
Average Pin = (2 P_B1 + Ptx) / 3 = (-92 – 27)/3 = -39.67dBm
IIP3 = 0.5(Pin – IM3) + Pin = 0.5 (-39.67 + 101.2) -39.67 = -8.9dBm

The IIP3 of the receiver can be relaxed by **1dB**.

Q3. This question is intended to calculate LO spur level requirement:

A PLL uses a 20MHz reference crystal oscillator that results in a reference spur +/-20MHz away from the LO used for a WCDMA receiver as shown below:



With the adjacent channel n+4 (or 20MHz away from desired signal) level of -40dBm, calculate the relative spur level in dBc (relative to the main LO) so that the folded n+4 signal in-band due to the PLL spur has a negligible impact on the receiver sensitivity of
-117dBm.

Answer:
For the direct-conversion receiver, the 20MHz blocker will mix with the spur folding the outcome in-band at baseband. For this outcome to have a negligible impact on sensitivity, the product of the blocker times this spur has to be at least 10dB below receiver noise (at sensitivity). Since at sensitivity we calculated receiver noise level of -99.2dBm → we will target -109.2dBm (10dB below)

Therefore, the baseband level = blocker level x spur level. Therefore with blocker level of -40dBm, and desired baseband outcome of -109.2dBm at antenna → spur level is (-109.2- (-40)) = **-69.2dBc**. Note that spur level is in dBc because desired signal is mixed with LO and blocker is mixed with spur, so if LO signal goes higher, desired signal goes higher and so the tolerated spur level goes higher as well since we always wanted the blocker level folding in-band to be 10dB below sensitivity noise (relative)

This means the spur level has to be >~70dB below LO level for this blocker not to impact sensitivity due to mixing with spur

Q4. This question is intended to refresh your RF matching knowledge to be ready for the following homework problems.

a. Let us assume an RF receiver block has an input impedance (Zin) of 10-ohms (real, no imaginary) at 2.5GHz. Design an L-match network to power match this impedance to a 50-ohm source. There are two possible ways to do an L-match; a series inductor followed by a shunt capacitor or a series capacitor followed by a shunt inductor. You need to design both if feasible. Assume the matching components are ideal (infinite Q). Plot S11 using Spectre. Also plot the matching network voltage gain (Vout @ the input ports of the DUT vs Vin @ the RF port terminal).

Answer:

1. Series inductor/shunt cap:

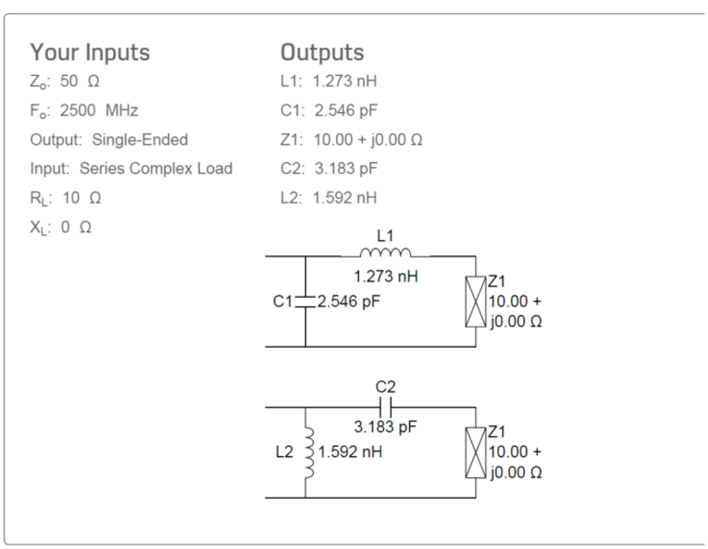
   Q = 2π*2.5e9*Ls /Rs=2π*2.5e9*Ls /10
   Q^2 + 1 = 50/10 → Q = 2
   ➔ Ls = 20/2π*2.5e9 = **1.27nH**

   Q = Rp/2π*2.5e9*Lp , (Rp = 50Ω, Q = 2)
   ➔ Lp = 1.59nH
   Csh = 1/[(2π*2.5e9)^2 x Lp] = **2.55pF**

2. Series cap/shunt ind:

   Q = 1 /(2π*2.5e9*Cs*Rs)= 1 /(2π*2.5e9*Cs*10)
   Q^2 + 1 = 50/10 → Q = 2
   ➔ Cs = 1 /(2π*2.5e9*2*10)= **3.18pF**

   Q = Rp*2π*2.5e9*Cp, (Rp = 50Ω, Q = 2)
   ➔ Cp = 2.55pF
   Lsh = 1/[(2π*2.5e9)^2 x Cp] = **1.59nH**



b. Replace the ideal inductors in your matching network in (a) with finite Q inductors (Q=10 to mimic on-chip spiral inductors, assume finite Q is mainly due to series resistance of inductor winding).With the aid of Spectre, re-simulate your matching network in (a). Feel free to "tweak" the components of your matching network to get a good S11 (<-12dB). Re-plot S11 and matching network voltage gain.

c. If the RF block impedance has additional capacitive reactive component of –j50 (so total input impedance is 10-j50 ohms), re-design your matching network to match this to a 50-ohm source. See if both L-match ways are still possible. Use ideal components first. Report S11 and matching network voltage gain. Repeat this step with inductor Q of 10.

Answer:

1. Series inductor/shunt cap:

   Adjust series Ls value to resonate with –j50 imaginary part of Zin. This additional series value = 50/(2*π*2.5e9) = 3.18nH
   ➔ Ls = 1.27nH + 3.18nH **= 4.45nH**

   The rest of calculation remains same

   Q = Rp/2π*2.5e9*Lp , (Rp = 50Ω, Q = 2)
   ➔ Lp = 1.59nH
   Csh = 1/[(2π*2.5e9)^2 x Lp] = **2.55pF**

2. Series ind/shunt ind:

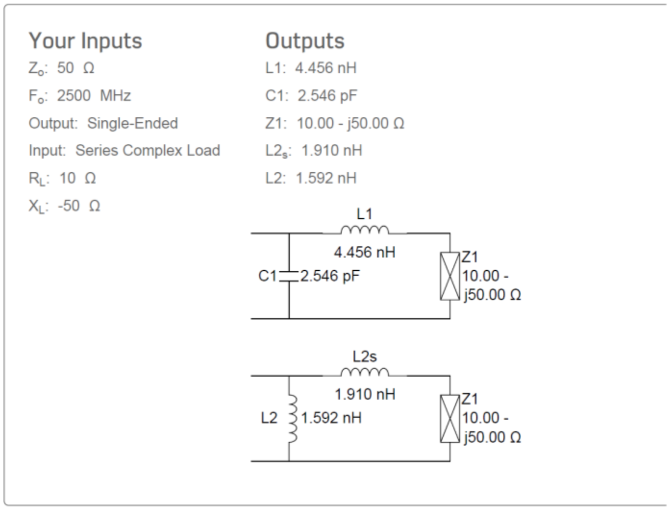
   -j50 = 1 /(2π*2.5e9*Css) → Css = 1.27pF

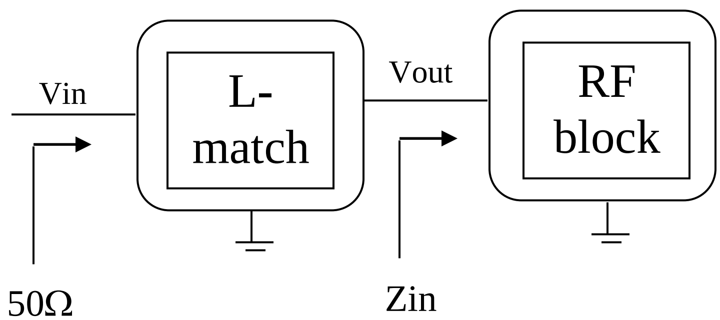
   However, we need to have an effective series capacitance of 3.18pF
   1/(2π*2.5e9*Cs) = 1/(2π*2.5e9*3.18e-12) = -j20

   This means we need to add a series inductor with impedance of j30
   ➔ 2π*2.5e9*Lss = 30
   ➔ Lss = **1.91nH**

   The rest of calculation remains the same
   Q = Rp*2π*2.5e9*Cp, (Rp = 50Ω, Q = 2)
   ➔ Cp = 2.55pF

   Lsh = 1/[(2π*2.5e9)^2 x Cp] = **1.59nH**


Your Inputs
Z_o: 50 Ω
F_o: 2500 MHz
Output: Single-Ended
Input: Series Complex Load
R_L: 10 Ω
X_L: -50 Ω
Outputs
L1: 4.456 nH
C1: 2.546 pF
Z1: 10.00 - j50.00 Ω
$L2_s$: 1.910 nH
L2: 1.592 nH
L1
4.456 nH
C1
2.546 pF
Z1
10.00 -
j50.00 Ω
L2s
1.910 nH
L2
1.592 nH
Z1
10.00 -
j50.00 Ω


Vin
L-
match
Vout
RF
block
50Ω
Zin