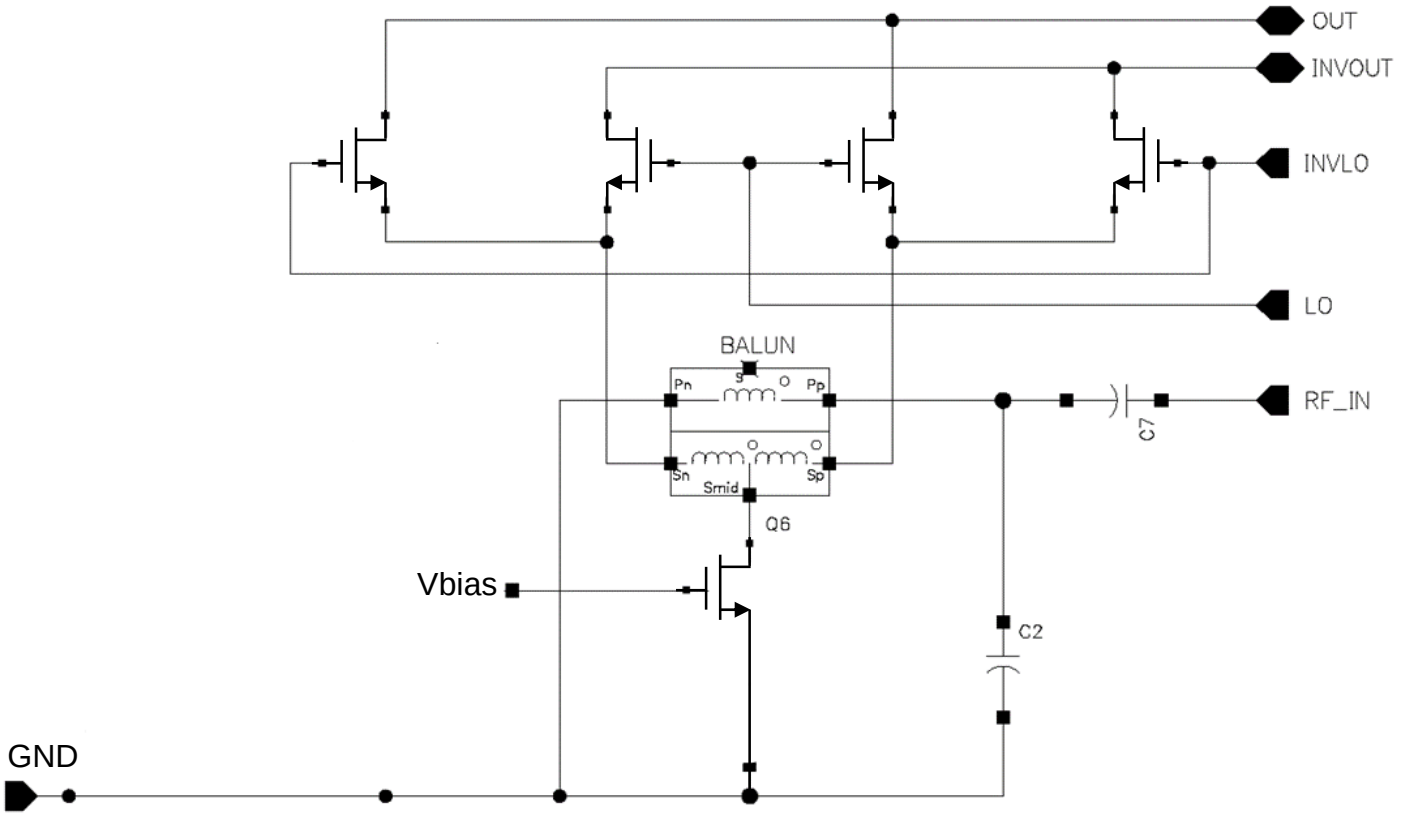
RF Mixer circuits

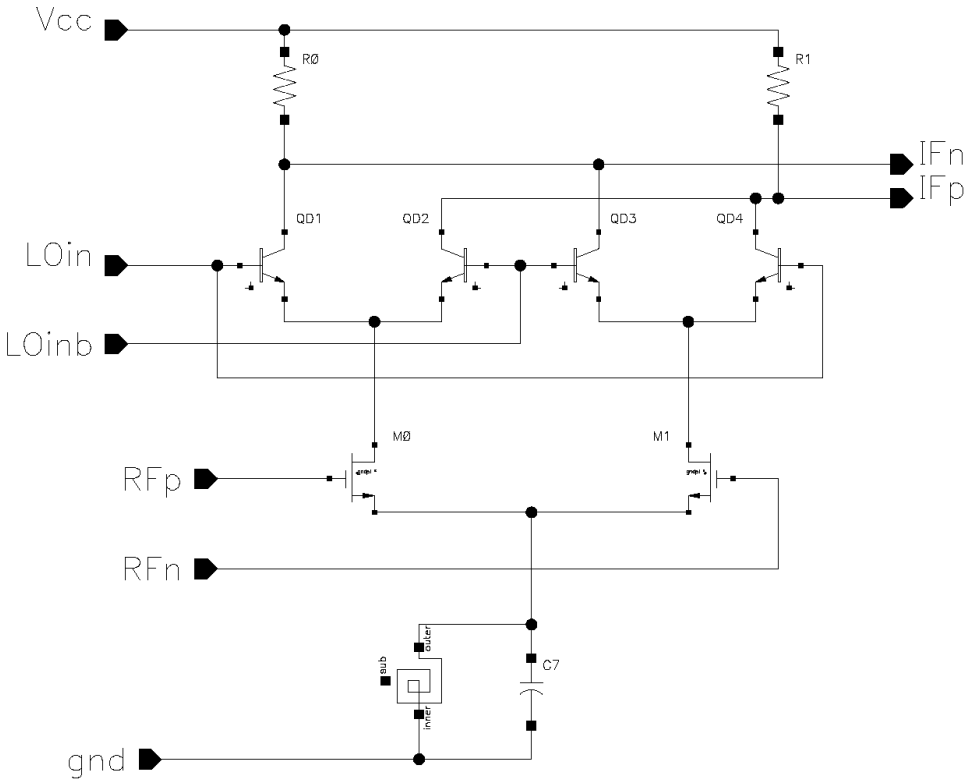
- **Mixer design**
  - Passive-Gm mixer
  - BiCMOS mixer
  - Passive mixers
  - Subharmonic mixers
  - LO buffers
- **References**

High IP3 low current passive Gm cell Gilbert mixer:



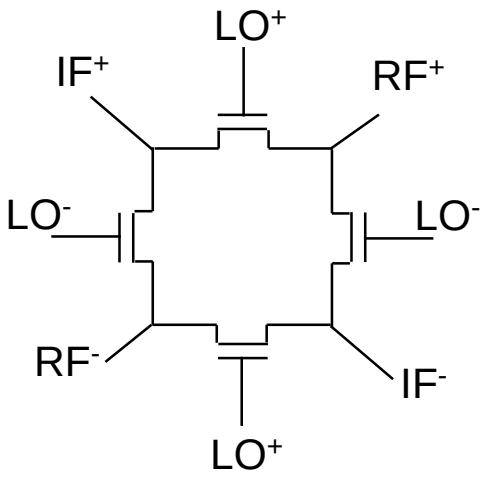
The passive Gm stage results in high IP3 for very low current (1mA or so) [2]. The NF, however, is relatively large, 12dB or so because of the balun loss as well as “unshielded” quad channel noise from the input.

High IP3 BiCMOS mixer:



CMOS Gm cell has a high IP3 for a given current compared to bipolar with small or even no degeneration. The bipolar quad will ensure low 1/f noise at the output and fast switching for good IP2 and IP3. Note that the Gm cell 1/f noise gets upconverted by the quad away from the baseband output. Such mixer can have an IP3 of +10dBm with <4mA of current at a gain of 10dB at 2GHz.

Passive MOS commutator:

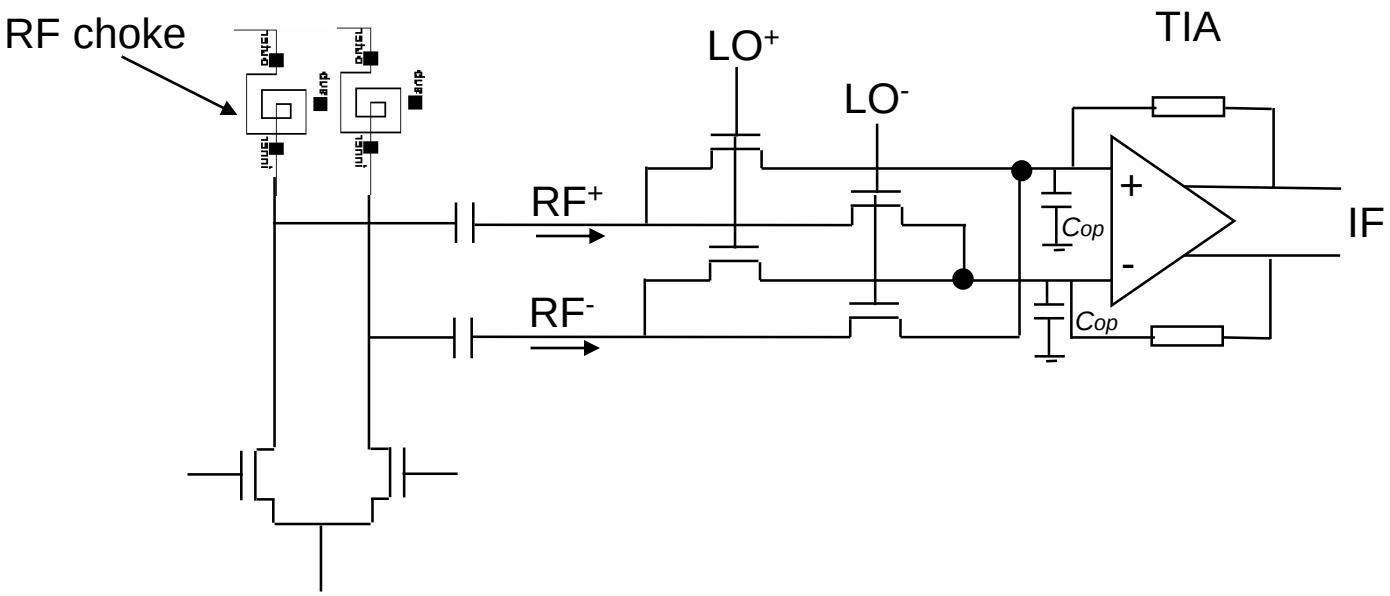


Transistors act as variable resistors as a function of LO

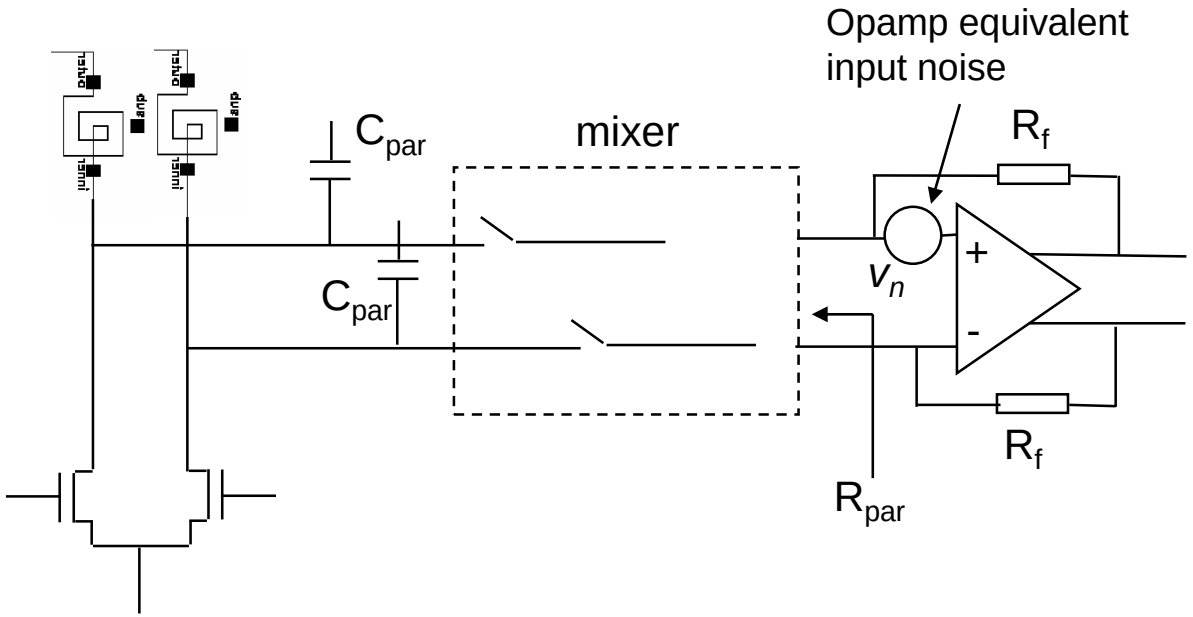
The advantages of the passive MOS commutating mixer:
- very good linearity
- zero current consumption
- no 1/f noise (no DC current)
- small area

The disadvantages
- no gain, rather it has loss ranging from 4~6dB
- large required LO drive, almost rail to rail (power consumption!)

Current commutating passive mixer circuit:



- LNA output RF current is fed into the passive mixer
- no DC current in passive mixer results in low 1/f mixer noise
- virtual ground of opamp improves overall linearity since mixer output (and associated nonlinear parasitic caps) does not swing in such configuration (*Cop* is added to shunt high-frequency mixing components of RF+LO)
- mixer device sizing for min loss and acceptable LO drive.
- opamp is designed and device sized for best 1/f noise corner



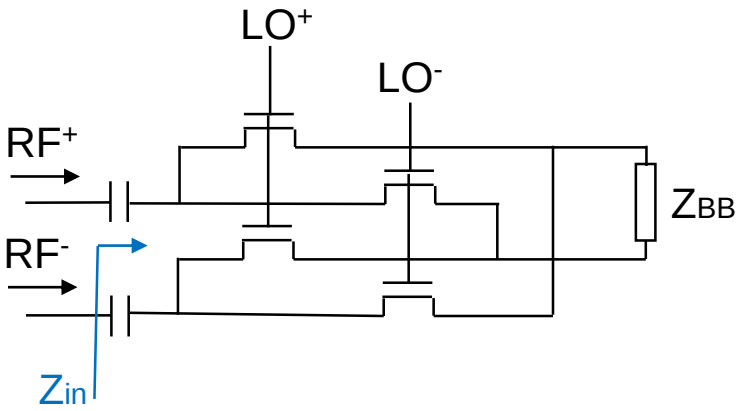
● the parasitic capacitor at the mixer input (due to mixer itself, LNA out, or layout) results in an effective switched-capacitor resistor due to the mixer switching action. The value of this resistor is

$$R_{par} = \frac{1}{4\pi f_{LO} C_{par}}$$

● the noise of the opamp gets gained up to the output by: $v_{n\_opamp\_out} = \left(1 + \frac{R_f}{R_{par}}\right) v_n$

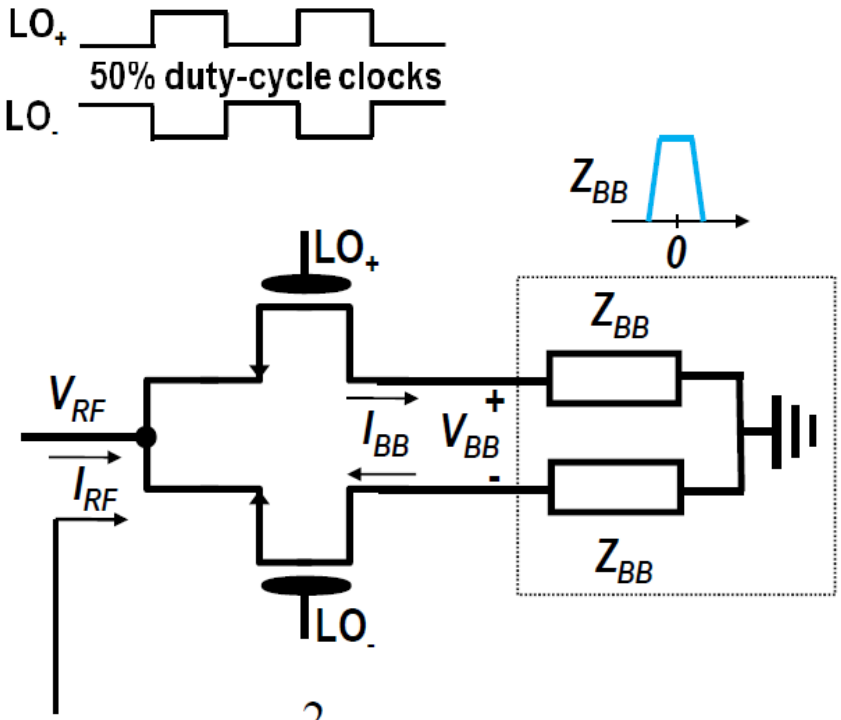
● to minimize this noise, the LNA inductive load must be designed to resonate with all parasitic capacitors at the mixer input to provide high impedance.

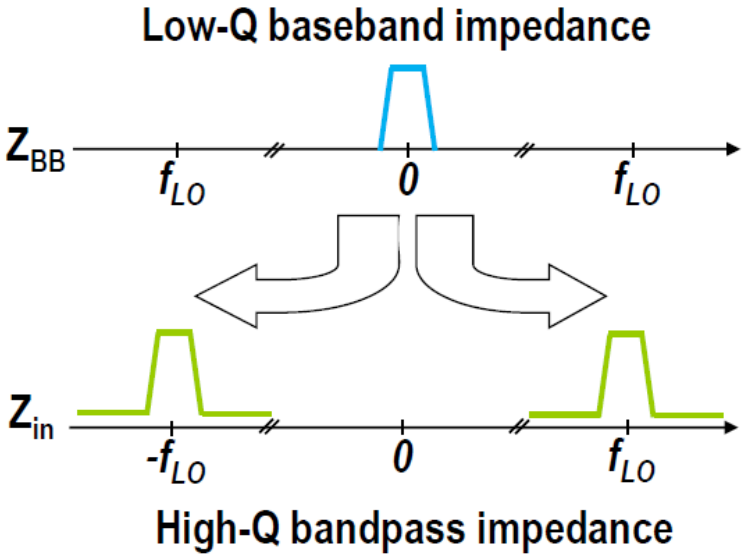
The bi-directional transparency nature of passive mixers:



- the passive mixer has “poor” isolation between RF and IF ports (RF and IF ports are shorted together when mixer device is on)
- in such condition the RF port “sees” a flavor of the baseband port impedance and vice-versa (bidirectional transparency)
- it turns out one can take “advantage” of such feature as analyzed next.
- such feature also can cause “harm” to the receiver (and transmit) design if not well taken care of

impedance transformation in passive mixers:



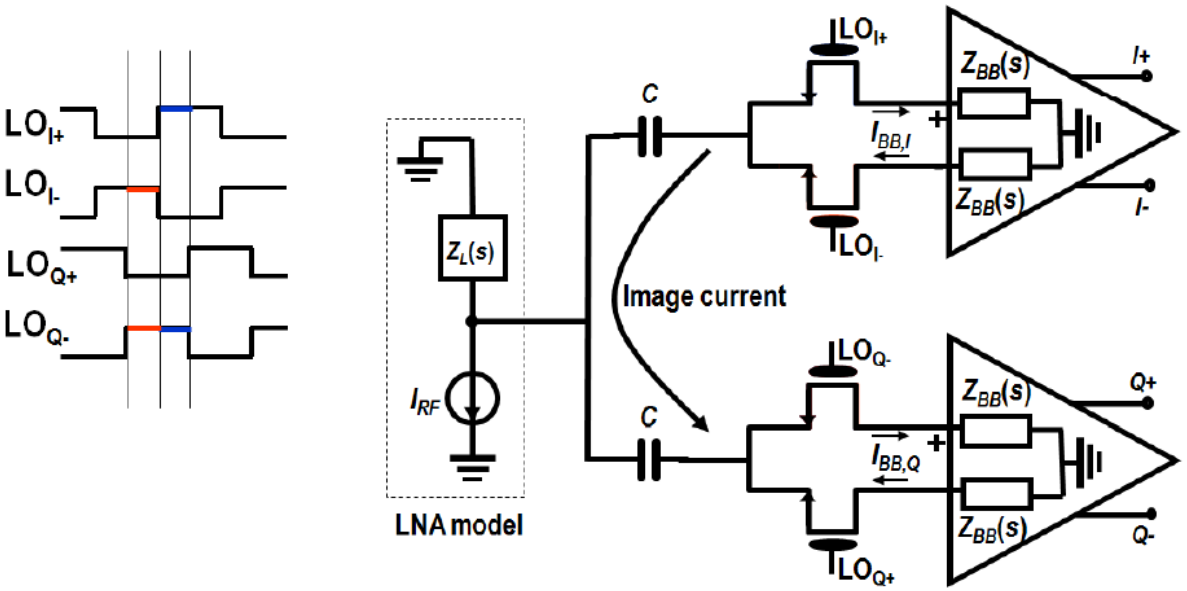


$$Z_{in} \cong R_{SW} + \frac{2}{\pi^2}\{Z_{BB}(s - j\omega_{LO}) + Z_{BB}(s + j\omega_{LO})\}$$

Mirzaei et. al JSSC 2009

- baseband impedance gets frequency shifted to RF centered at LO frequency creating a high-Q RF filter!
- the center of that RF filter is controlled by LO PLL

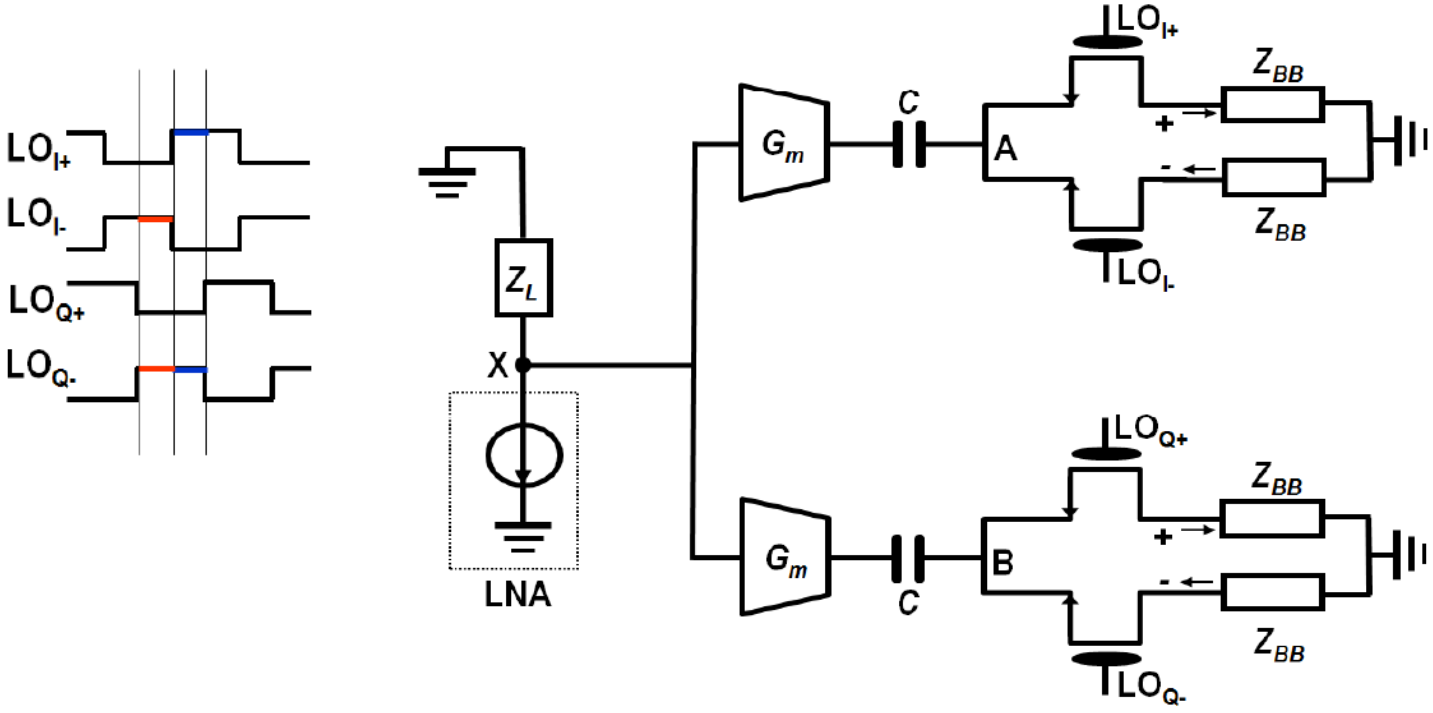
The I/Q cross talk and its impact on passive mixers:



[7] Mirzaei et. al JSSC 2009

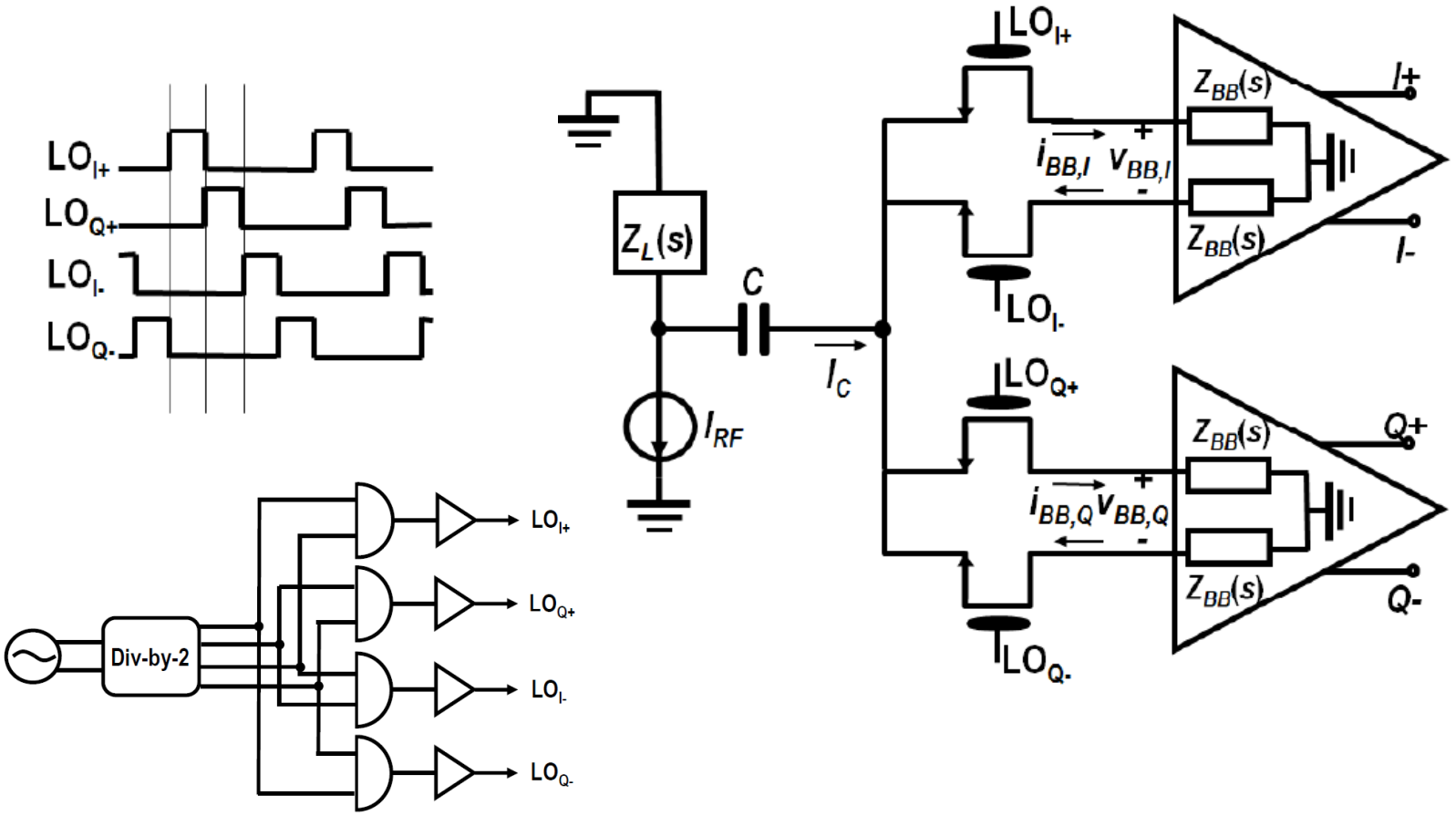
- Because of the overlapping I/Q 50% duly-cycle LO, the I-port will see the Q-port and visa-versa resulting in I/Q cross-talk
- The cross talk results in several unwanted performance degradation such as:
  - Different linearity (IP3/IP2) between I and Q ports
  - Different mixer gain between upper/lower mix
  - Degraded receiver NF

How to solve the The I/Q cross talk in passive mixers:



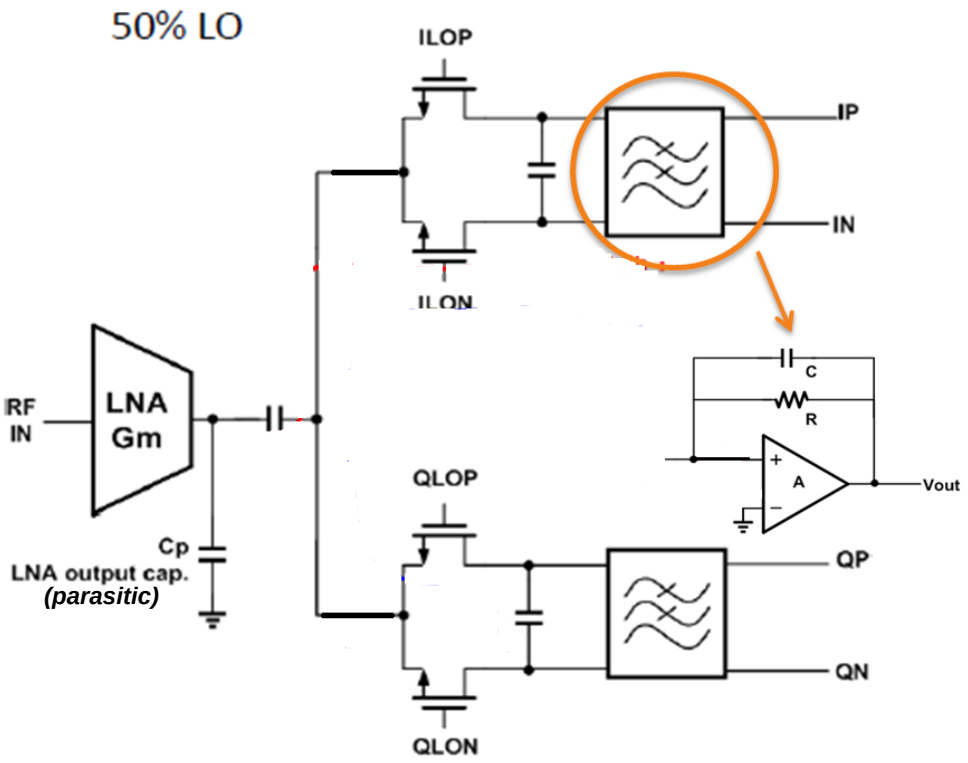
- Inserting an RF Gm stage in series with I and Q brach helps block the image current, hence the cross talk
- Side effect of this approach is degraded linearity and noise plus extra current and die area

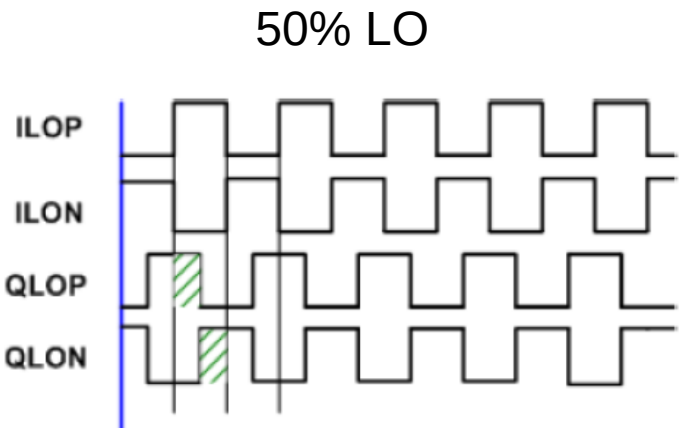
25% LO to solve the The I/Q cross talk in passive mixers:



- Only one mixer switch ON at any given time → better I/Q isolation
- No linearity impact
- Overhead circuits in generating 25% LO (extra current)

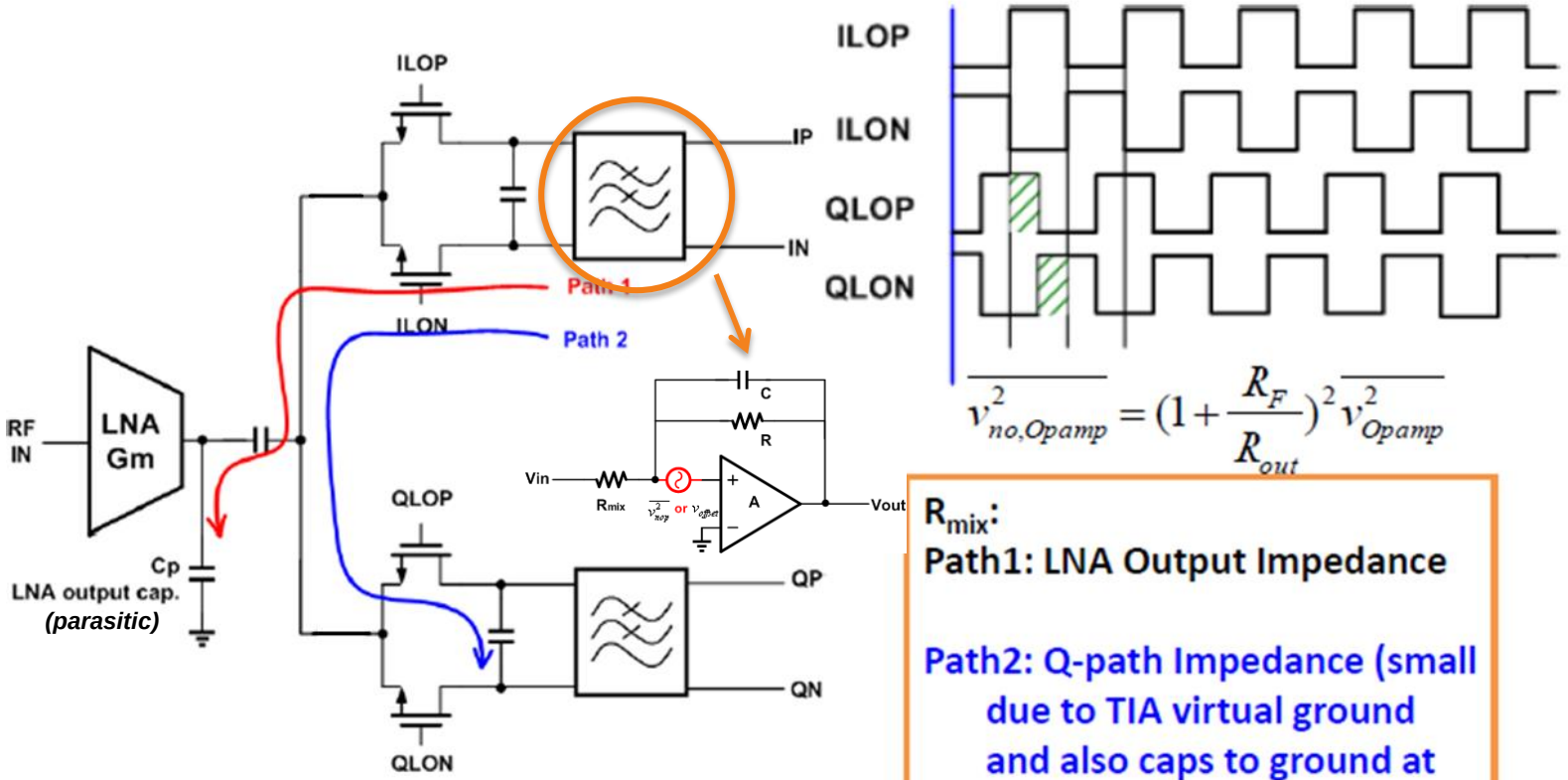
A real example of a passive mixer-based receiver:





- current-mode LNA with opamp as TIA is one of the most popular receiver topologies due to high-linearity, low Vdd and low current
- Simulated NF for this receiver with 50% LO and NF was BAD → why?

Opamp noise amplification due to 50% LO overlap:



$$\overline{v_{no,Opamp}^2} = (1+\frac{R_F}{R_{out}})^2 \overline{v_{Opamp}^2}$$

R_{mix}:
Path1: LNA Output Impedance

Path2: Q-path Impedance (small due to TIA virtual ground and also caps to ground at TIA inputs)

→ High gain of opamp noise

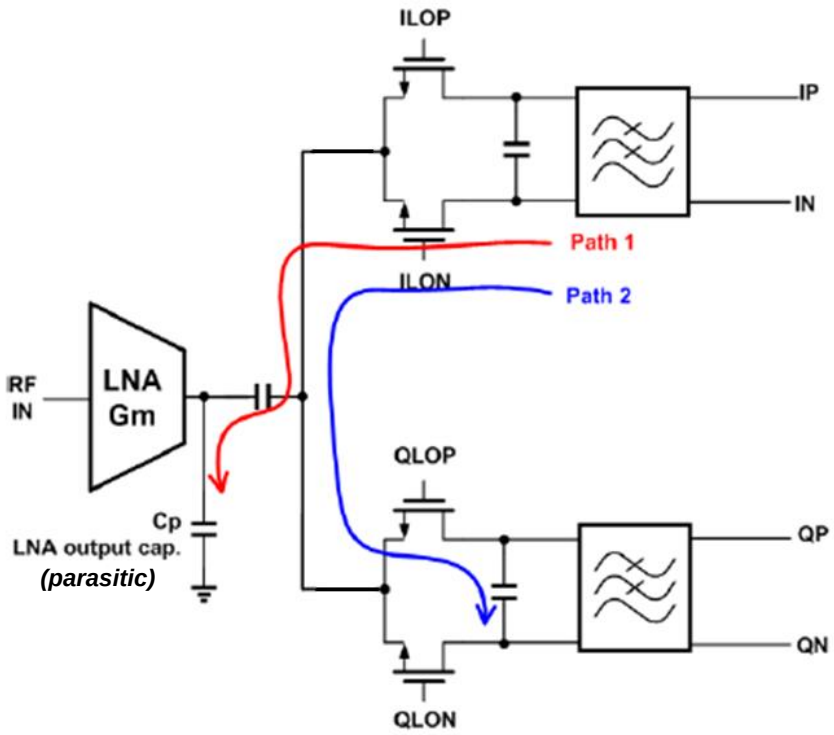
$$\overline{v_{nop,out}^2} = \overline{v_{nop}^2}(1+\frac{R}{R_{mix}})^2$$

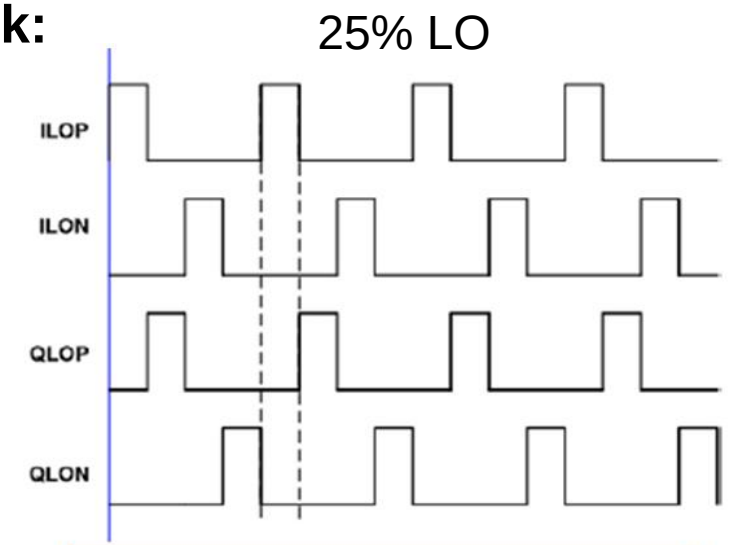
$$v_{offset,out} = v_{offset}(1+\frac{R}{R_{mix}})$$

Larger Rmix → Better DC offset and Noise

- With 50% LO, opamp noise is dominant due to I path seeing Q virtual ground due to LO overlap

25% LO to solve the The I/Q cross talk:





Path 2 is high impedance for Non-overlapping LO

Opamp noise amplification effect depends only on LNA output impedance, which is relatively high
→ Relatively low gain for opamp noise

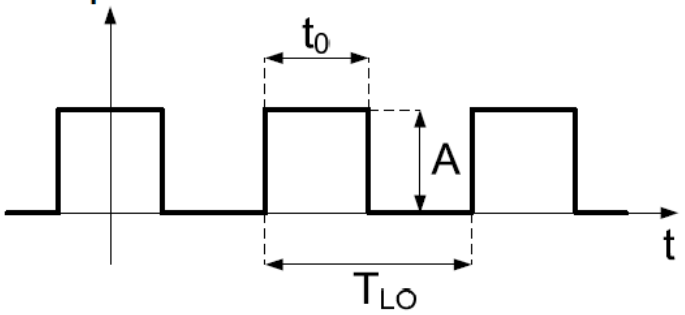
- NF is back to normal when using 25% LO (overlap is gone)
- However, gain suddenly went up by 3dB compared to 50% LO case → why?

How to explain gain difference by just changing LO duty cycle:

- IF = RF x LO
- RF component is up by 6dB with LO going from 50% → 25% because no more RF current splitting between I and Q
- What happens to the LO component when going 50% to 25%?

❑ The Fourier coefficients of a square wave are:

$$C_n = \left[2A \frac{t_0}{T_{LO}} \frac{\sin\left(\frac{n\pi t_0}{T_{LO}}\right)}{\pi n \frac{t_0}{T_{LO}}} \right]$$



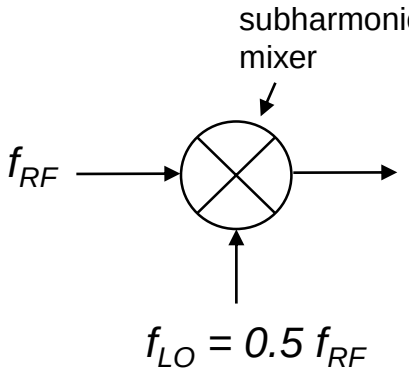
(where n is the harmonic number, t_0/T_{LO} is the LO mark-space ratio and A is the mixer output amplitude)

❑ If n=1 and t_0/T_{LO}=1/4, the duty cycle is 25% : $C_1 = \frac{2}{\pi} \times \frac{1}{\sqrt{2}} A$

❑ If n=1 and t_0/T_{LO}=1/2, we get a 50% duty cycle (as in a conventional mixer): $C_1 = \frac{2}{\pi} A$

↳ Therefore, we have a loss of amplitude at the fundamental frequency by a factor √2 by using the 25% duty cycle LO instead of the 50%.

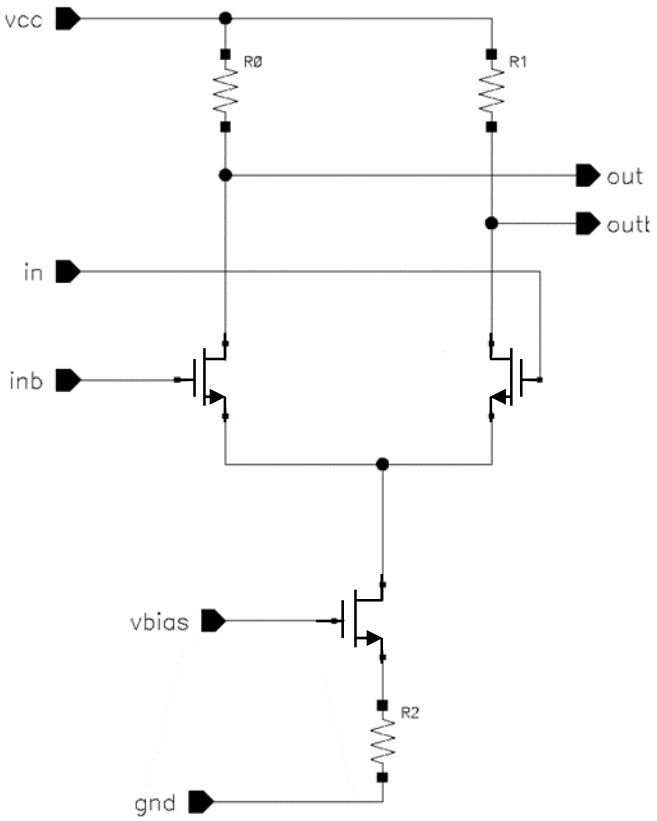
Subharmonic mixer design:



The subharmonic mixer is driven by an LO signal that is an integer fraction, or subharmonic, of the desired LO frequency. For example, if the RF signal is 2GHz, and the desired LO is 2GHz for direct conversion, a subharmonic mixer will be driven by a 1GHz LO signal. The advantages are:

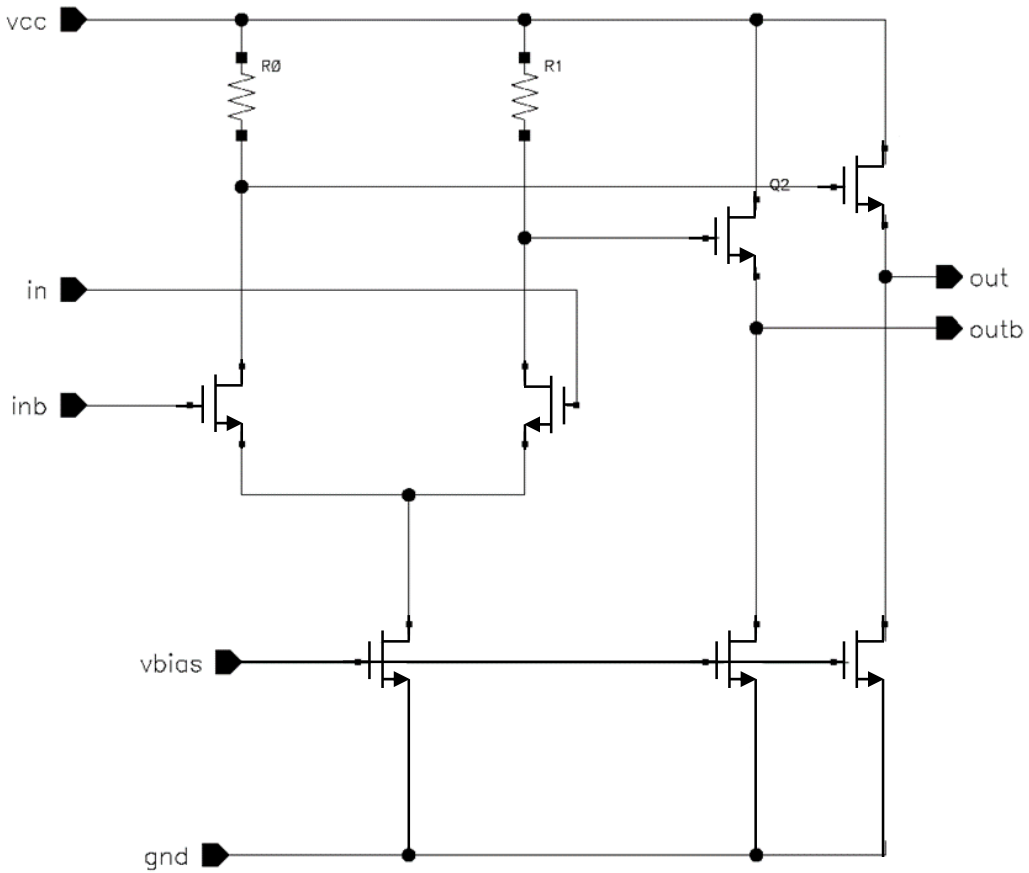
1. Lower LO re-radiation through the antenna (LO leakage)
2. lower LO self mixing (lower DC offset at IF)
3. Relaxed requirement on the device switching speed.
4. Lower LO buffer current

LO buffers:

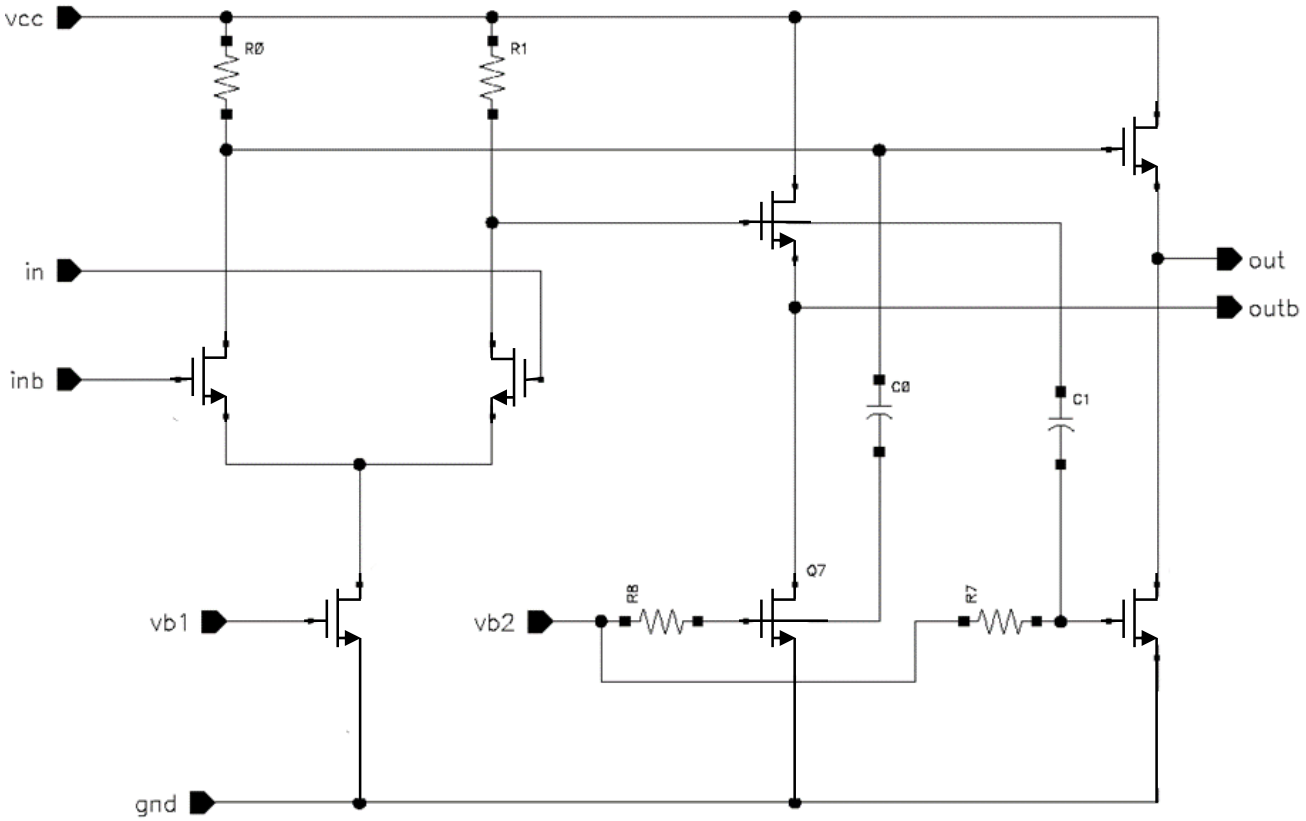


***Always** design/size the mixer switching transistors in conjunction with LO buffer design!*

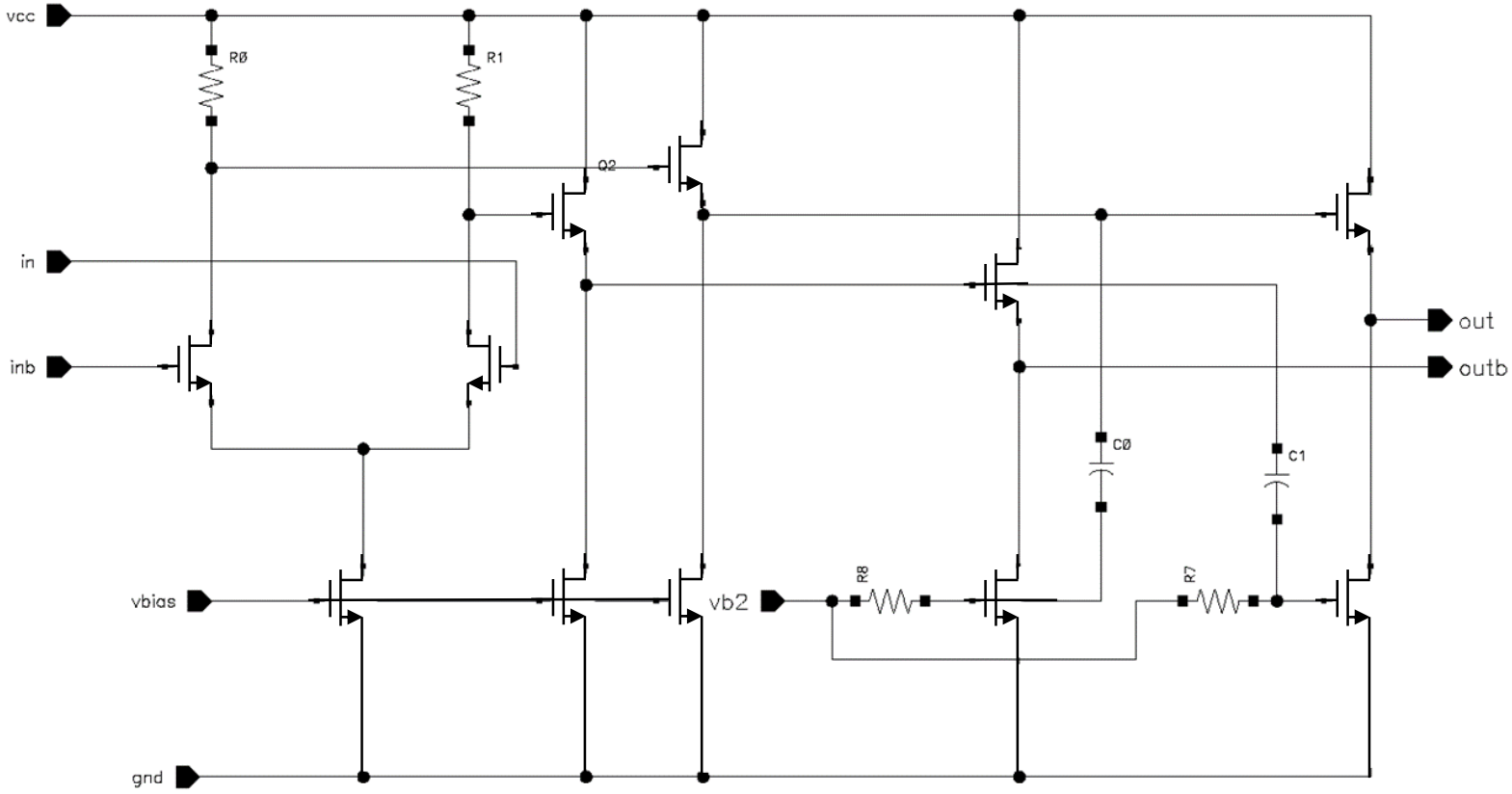
It is evident by now that the LO signal “shape” highly impacts the mixer linearity and noise. The goal is to achieve as close to a square wave LO as possible. The above is a simple way to “square” an LO signal. However, the rise and fall time is severely limited by the RC time constant of the LO squaring circuit load and the mixer input quad capacitance.



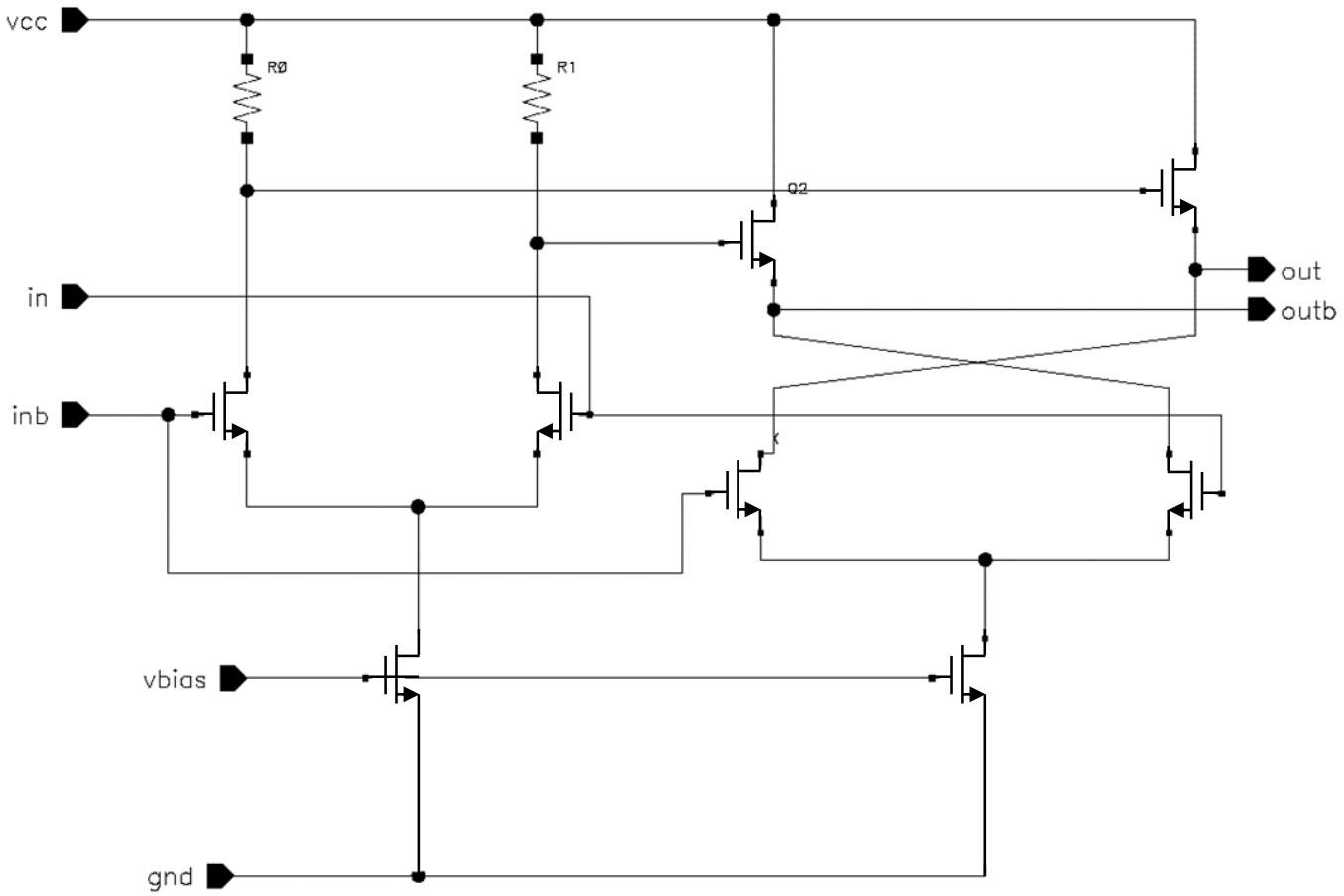
An source-follower following the limiter circuit provides a low-impedance to drive the large mixer quad devices. However, the fall time will be limited by the source follower current source in discharging the quad capacitance. This means to achieve sharp fall time, more current needs to be used to bias the source followers.



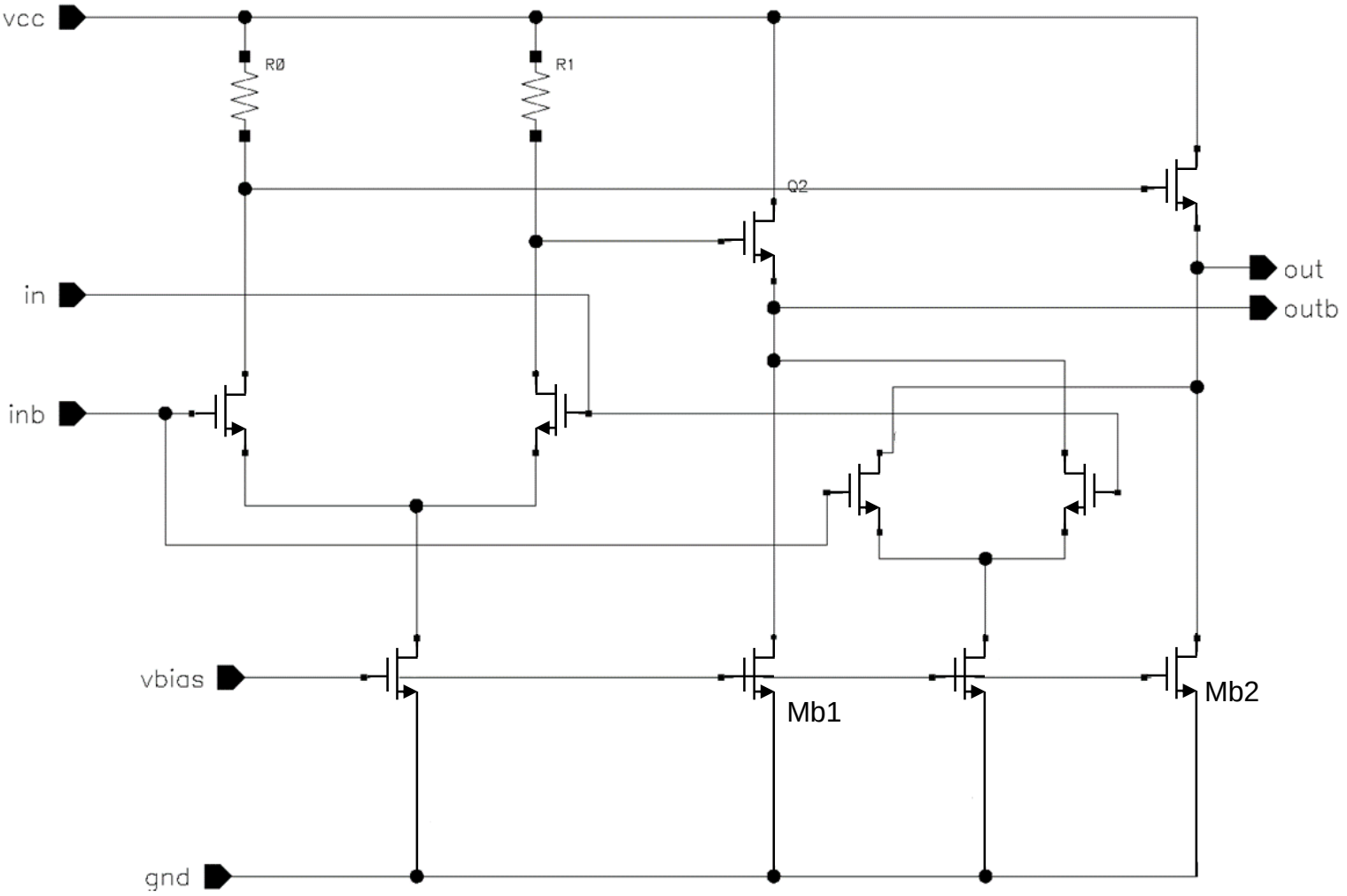
In order to reduce power consumption and make the LO buffer more efficient, some push-pull technique is required. Therefore a push-pull buffer is used as shown above. The out of phase signal is capacitively coupled to the gate of the current source to increase its current during falling edge. The time constant of the load R and the coupling cap C limits both rise and fall time.



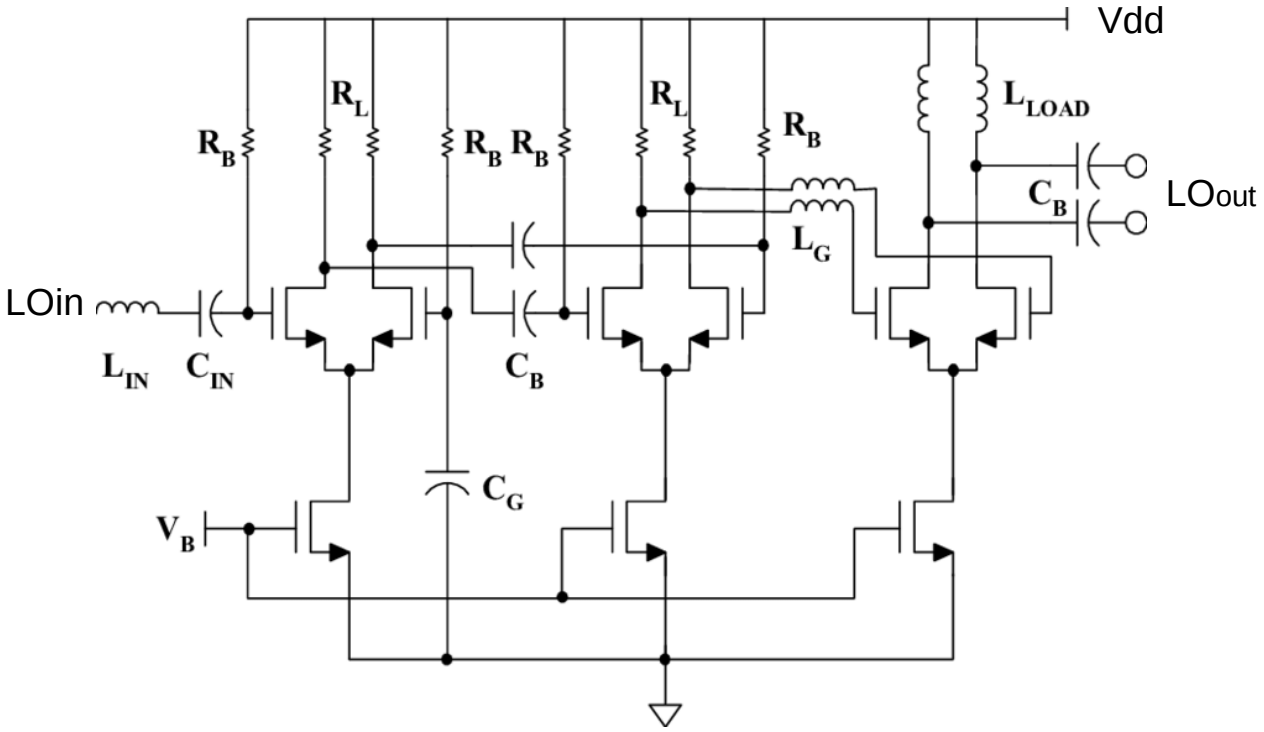
An improved push-pull buffer uses source followers to shield push-pull coupling cap from the limiter load. This circuit can achieve real sharp rise and fall time in the range of 10~15V/ns



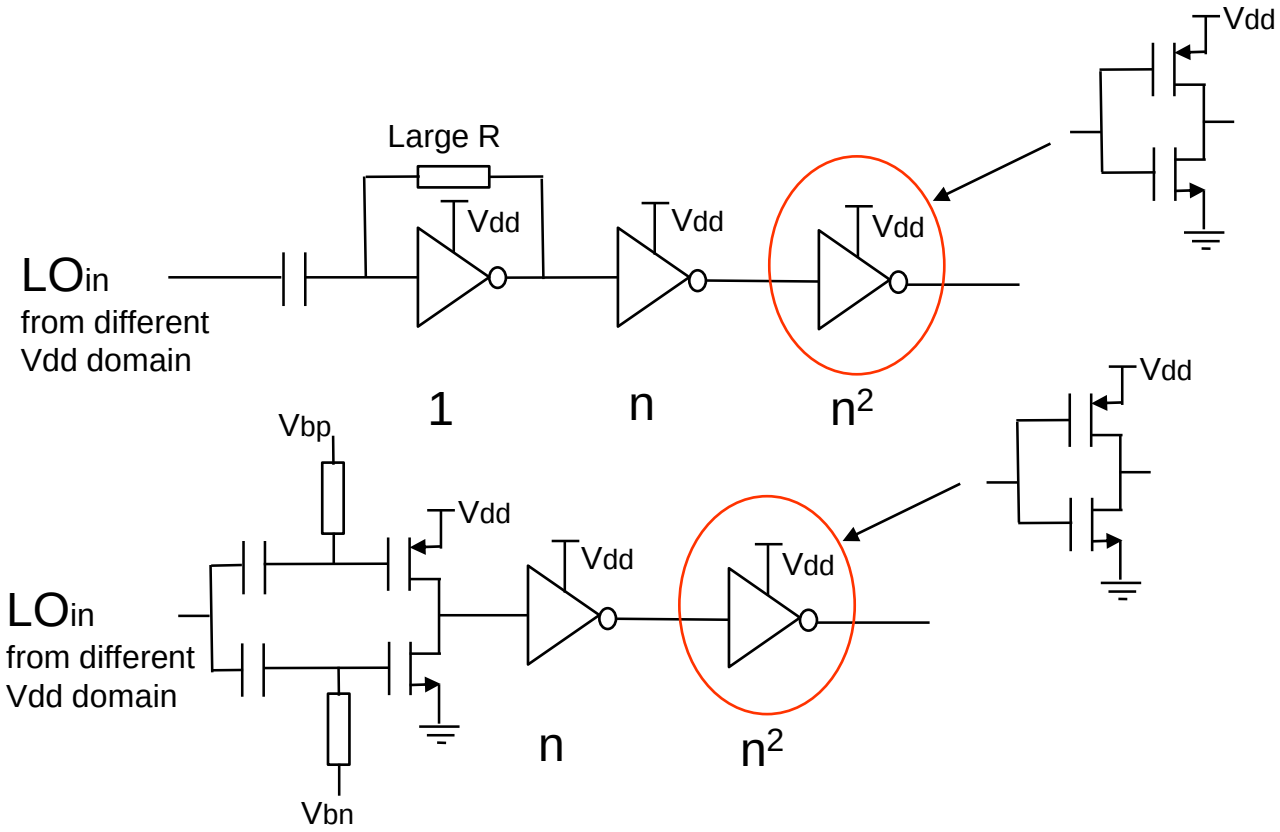
An active push-pull can also be used. The principle is to move the DC current from the “rising” branch to the “falling” branch, where it is needed the most. Note that this circuit is prone to oscillation If not carefully designed. This is because the 1/gm load of the push-pull gets larger as the current is steered to one side.



A bleed current, Mb1/Mb2 can be used to limit the 1/gm load of the active push-pull. The output of this circuit is plotted next.

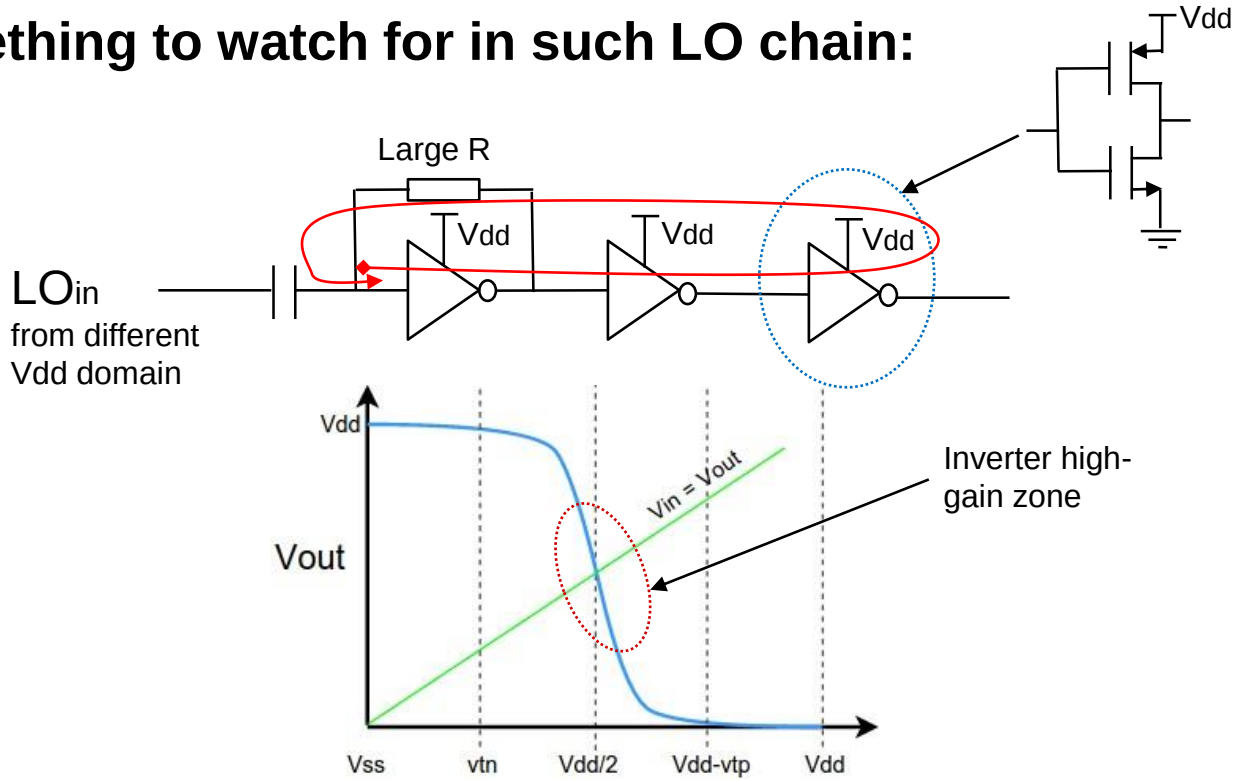


- Inductive load LO buffer provides the advantage of large LO swing (can swing above Vdd). It also has lower LO harmonics due to load LC tank
- Popular LO buffer for long LO routing at high frequency (say 10GHz).
- In many cases, bottom current source is removed so the stage can operate class-C
- Also sometimes a cascode stage is added to help with the Miller effect
- L_G in the schematic is not needed most of the time if frequency is <10GHz
- L_{LOAD} is usually implemented as a differential inductor to save area and improve Q



- An AC coupling plus a self-biased inverter stage are needed to center the coming LO signal swing around the proper DC point for the LO buffer Vdd (VERY important)
- Another topology is to AC couple both nmos and pmos devices of first stage buffer and independently bias these devices for better buffer strength
- LO buffer chain number of buffer stages and device sizing is optimized based on load cap, frequency and CMOS process node

Something to watch for in such LO chain:



- There is a large DC gain around this chain with a feedback path via Vdd. If each stage as 20dB DC gain, this loop has 60dB gain → potential instability
- You make sure the Vdd port has low impedance at both DC (good LDO) and at high frequencies. Another way is to insert and RC-filter in each Vdd to reduce feedback gain and/or manipulate phase of the loop
- I have seen loops like this oscillate at few hundred MHz especially if LO input is weak (large LO swings moves you away from the high-gain region of these stages)

References:

[1] A. Pärssinen, J. Jussila, J. Ryynänen, L. Sumanen, and K. I. Halonen, "A 2-GHz wide-band direct conversion receiver for WCDMA applications," IEEE JSSC, vol. 34, pp. 1893-1903, December 1999.

[2] John R. Long, Miles A. Copeland, Peter Schvan, and Robert A. Hadaway, " low-voltage silicon bipolar RF front-end for PCN receiver applications," IEEE International Solid-State Circuits Conference, vol. XXXVIII, pp. 140 - 141, February 1995.

[3] J. C. Rudell, J. Ou, T. Byunghak, C. Chien, F. Brianti, J. Weldon, P. Gray, "A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications," IEEE JSSC, vol. 32, pp. 2071-2088, December 1997.

[4] M. Valla, G. Montagna, R. Castello, " A 72mW CMOS 802.11a Direct Conversion Front-End with 3.5dB NF and 200kHz 1/f Noise Corner," IEEE JSSC, Vol. 40, No. 4, April 2005, pp. 970-977.

[5] D. Leenaerts, W. R. White, "1/f noise in passive CMOS mixer for low and zero IF integrated receivers," *in Proc. 27th Eur. Solid-State Circuits Conf*. Austria 2001, pp. 103-107.

[6] Jan Crols, Michel S. J. Steyaert, "A 1.5 GHz highly linear CMOS downconversion mixer", IEEE Journal of Solid-State Circuits, vol. 30, pp. 736 - 742, July 1995

[7] A. Mirzaei, *et. al*., "Analysis and Optimization of Current-Driven Passive Mixers in Narrowband Direct-Conversion Receivers," IEEE Journal of Solid-State Circuits, vol. 44, No. 10, pp. 2678 - 2688, October 2009.