multi-mode LNA design
broadband LNA design
bipolar LNA design (appendix)

- **Low noise amplifier**
  - Dual-linearity LNA
  - Dual gain LNA
  - Practical consideration for LNA design
  - Broadband LNA
    - » Shunt-shunt LNA
    - » Noise-cancelling LNA
- **References**

LNA Design for dual Linearity

In some multi-mode wireless applications, there is often a need to vary the linearity required of the LNA during reception cycle. This usually happens in full duplex systems where the power amplifier (PA) of the transmitter is turned on during the receive cycle. An example for such a system is CDMA. In such narrow-band system, both the receiver and the transmitter share the same antenna. The Tx leakage power, although out-of-band, causes an in-band AM distortion, as discussed in earlier lectures, severely degrading the SNR of the entire receiver. Consequently, the LNA linearity may have to be increased depending on the relative distance between the user and the base station.

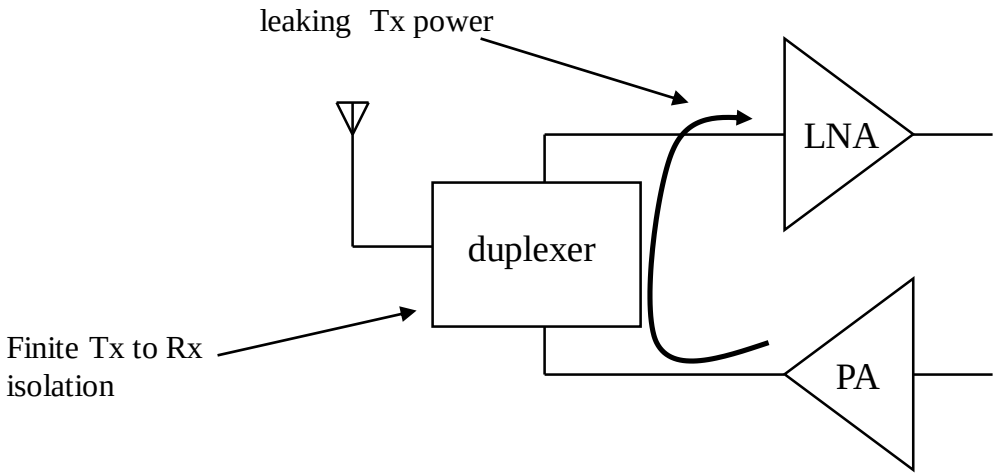
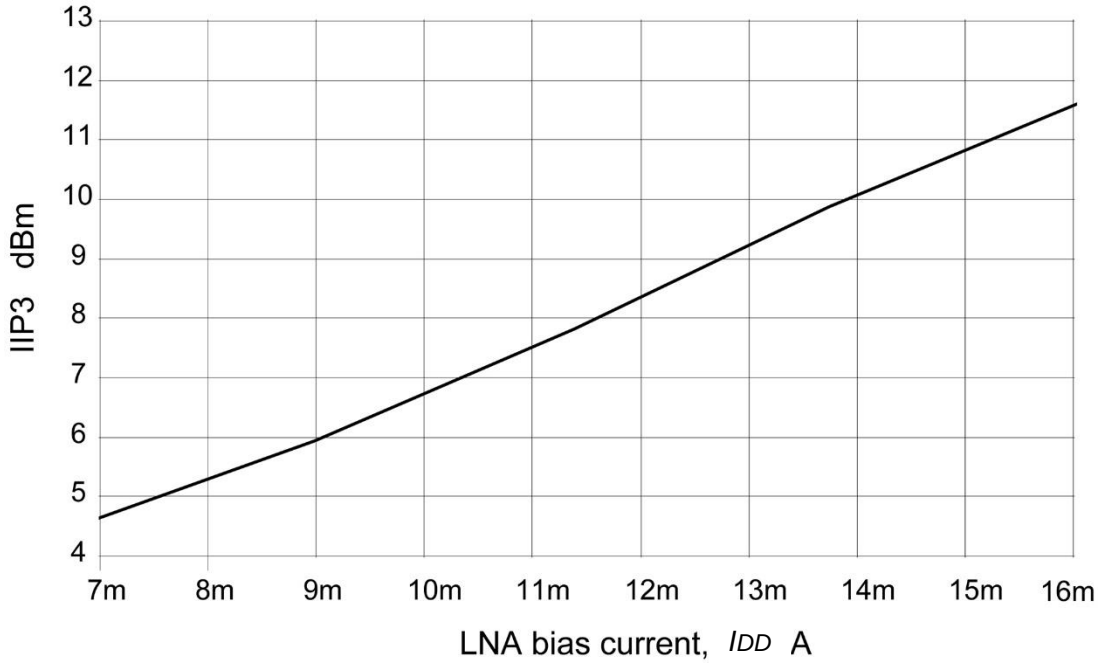
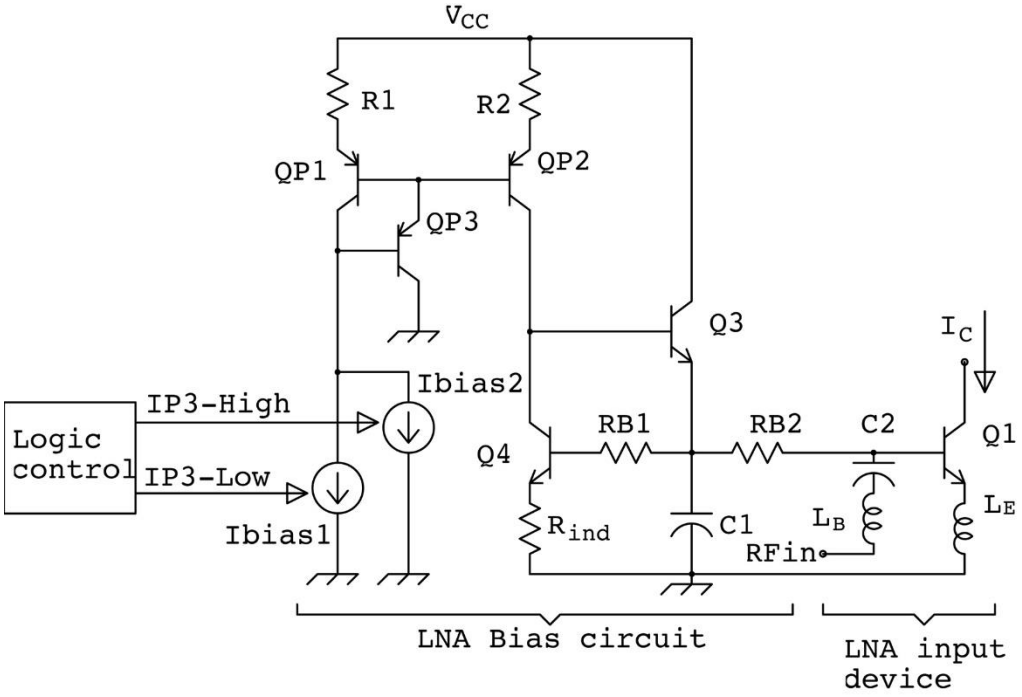


Fig. 4.10



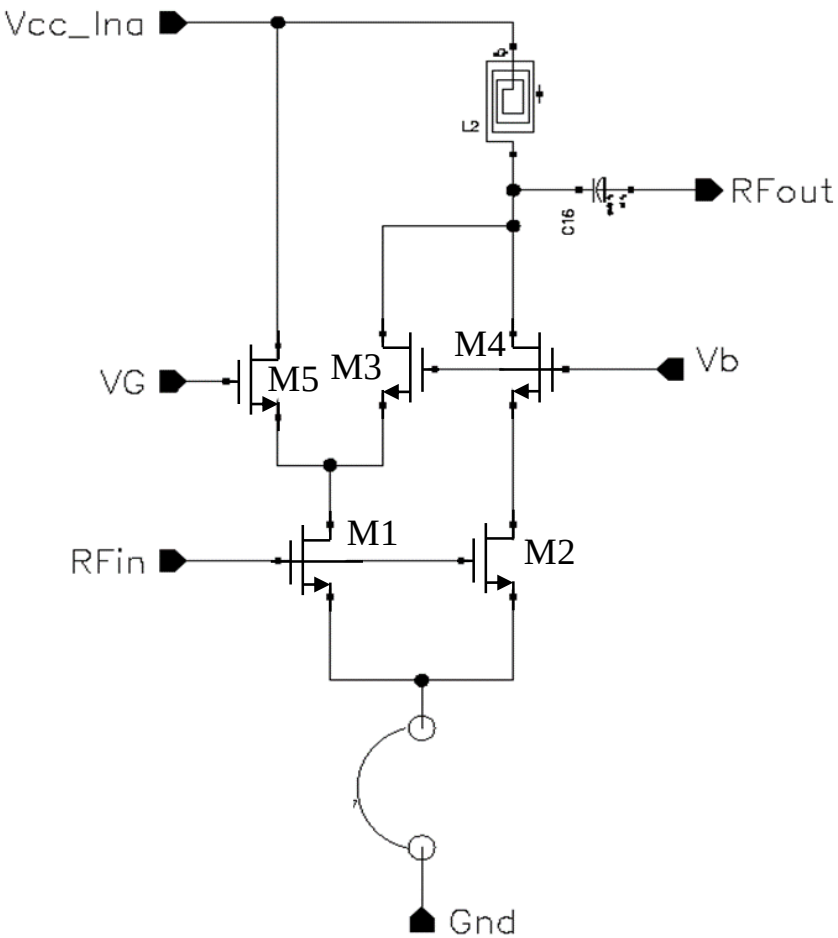
To increase the dynamic range of the LNA, basically the IIP3, the bias current of the LNA has to be increased. The IIP3 increases by roughly 6 dB if the bias current is doubled. In general, there are two to three different operational modes for such receivers depending on the desired gain and linearity of the LNA. We will consider only the modes where only the linearity has to be adjusted assuming a fixed desired gain. Because of LNA degeneration, the LNA gain changes slightly with changing I_{DD}.

A typical circuit setup to adjust the IIP3 of the LNA digitally is shown in Fig. 4.12. Here, the bias current of the LNA is increased when the high-linearity mode is desired. Because of the shallow nature of the optimum noise figure point, as seen in Fig. 4.5, doubling the bias current (and so the bias density) to increase the IIP3 of the LNA by 6 dB causes the LNA *NF* to increase by no more than 0.1 dB. This is quite crucial to keep the entire system *NF* within an acceptable level. Because the input impedance of the LNA depends on the f_T of the input device, increasing the bias current causes a degradation in the input match (the parameter S11). Need to ensure S11 remains <-10dB



Dual-gain LNA:

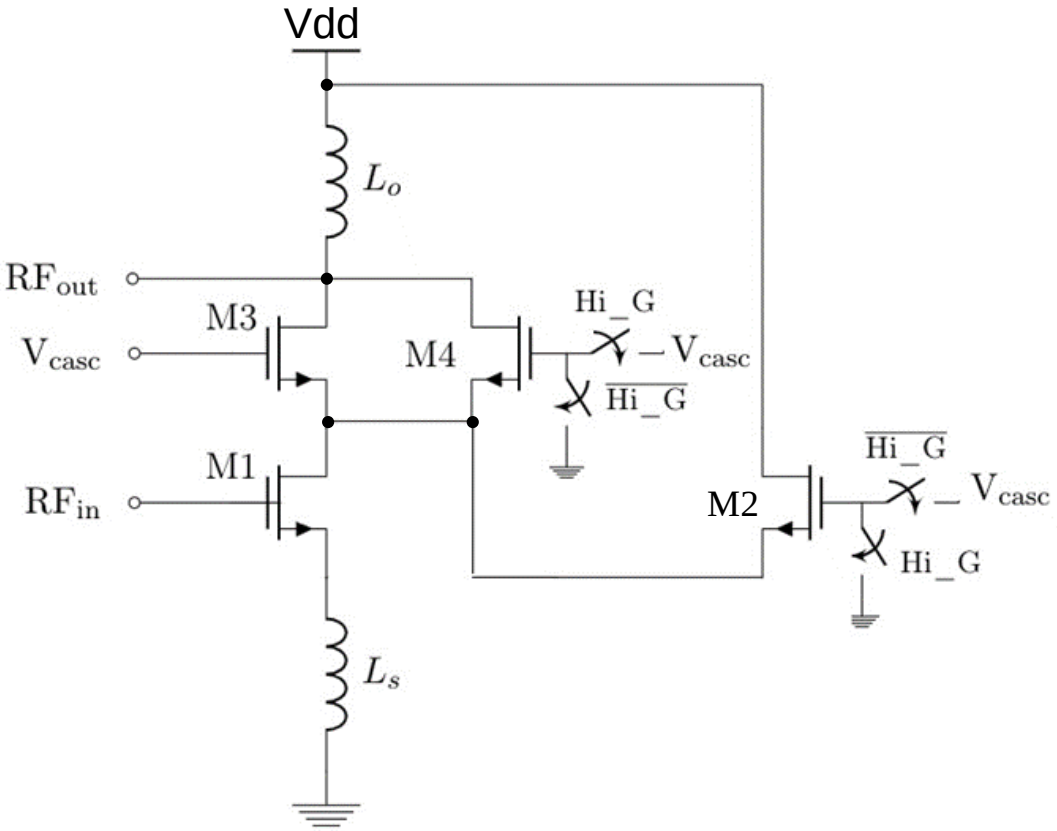
With the digital logic signal “VG” is low, M1,M2 and M3,M4 appear in parallel and so the LNA is in high gain mode. When VG is high, M5 turns on and steers away all the current of M3 to VCC and away from the load. Hence only a portion of the RF current reaches the output, and so the LNA is set to medium gain mode. The ratio between the gain in both modes equals that of the device ratio of M1 to M2.



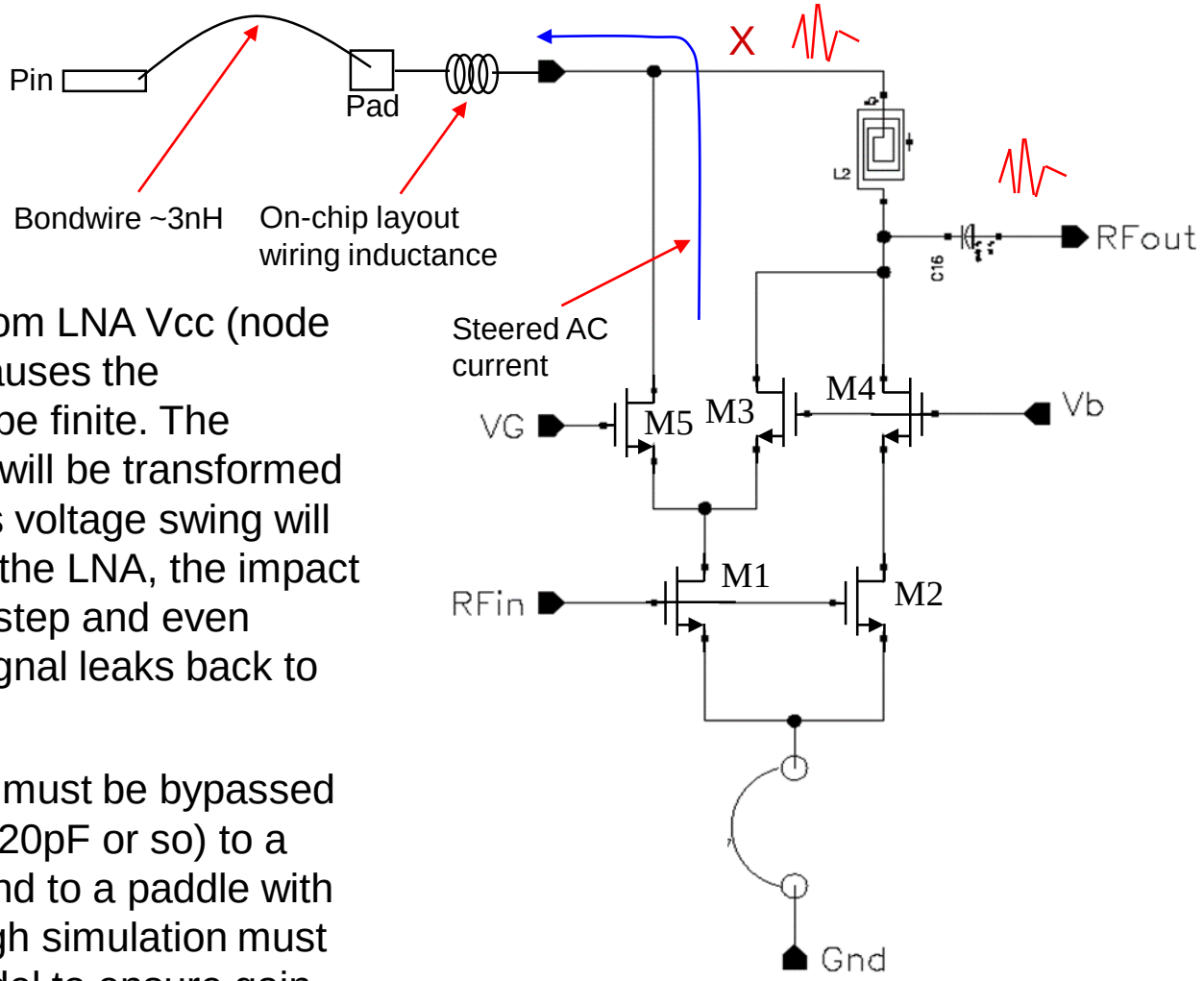
Note: maintaining good gain step accuracy over PVT is important in many systems to ensure overall Rx gain monotonicity and good SNR over AGC. Therefore, design LNA with gain steps that are process (and temp) independent as much as possible

Dual-gain LNA, cont':

Doing the current steering/slicing at cascode provides better noise increase vs gain step because the cascode device M3 noise contribution increase due to its channel noise flowing through M2 source (hence M3 channel noise is no longer circulating within M3) is still shielded from input by M1 transconductance. In this topology, M2 and M4 are of same size. The gain step is set by the device size ratio of M3 and M4 (M2).



Design consideration for current-steering type dual gain LNAs:

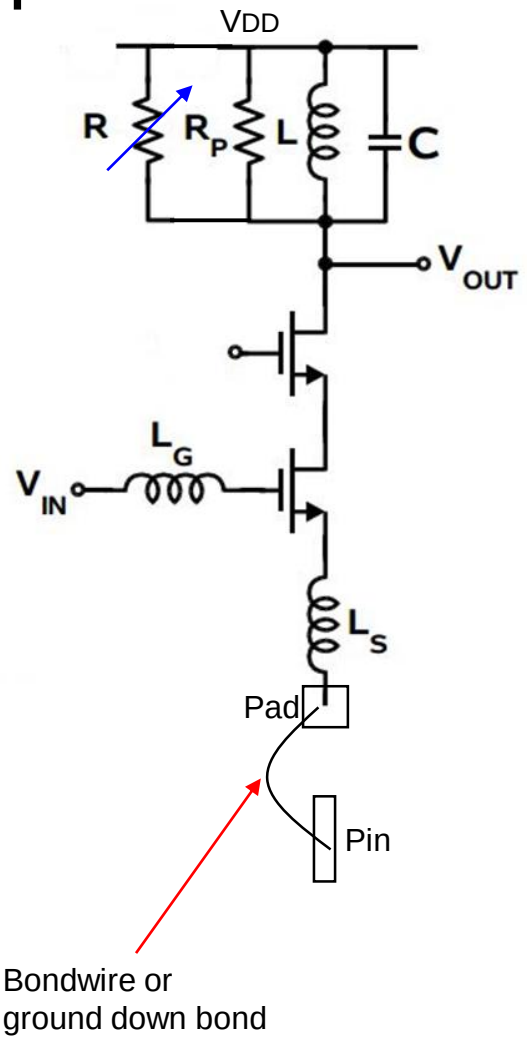


The parasitic inductance from LNA Vcc (node X) to actual LNA Vcc pin causes the impedance at that node to be finite. The steered current of the LNA will be transformed into voltage at node X. This voltage swing will be seen from the output of the LNA, the impact of which is a reduced gain step and even potential instability if this signal leaks back to LNA core.

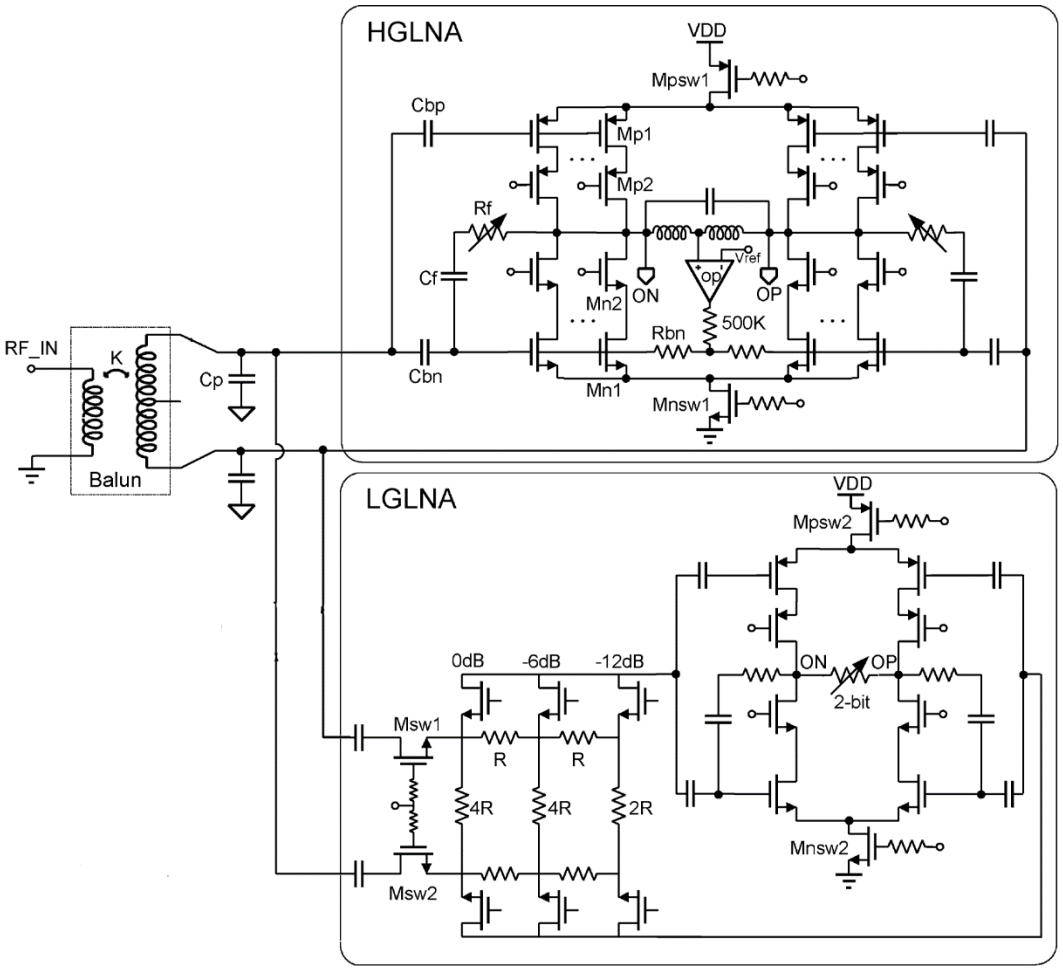
To fix this problem, node X must be bypassed through on-chip large cap (20pF or so) to a dedicated ground down bond to a paddle with lowest inductance. Thorough simulation must be made with package model to ensure gain step accuracy as well as LNA stability. A Vcc bypass capacitor at the Vcc pin is also needed.

LNA output load de-Q to implement gain step:

- A digitally controlled resistor bank “R” can be used to de-Q output load resonance, hence implement gain control
- Effective RL of LNA becomes Rp//R. Rp is set by inductor Q while R is set by poly-resistor variation over PVT → tracking over PVT is not perfect but is still ok
- Drawback is output compression becomes current-limited (not headroom limited) and so LNA compression can become input-limited (set by Vgs-Vt)



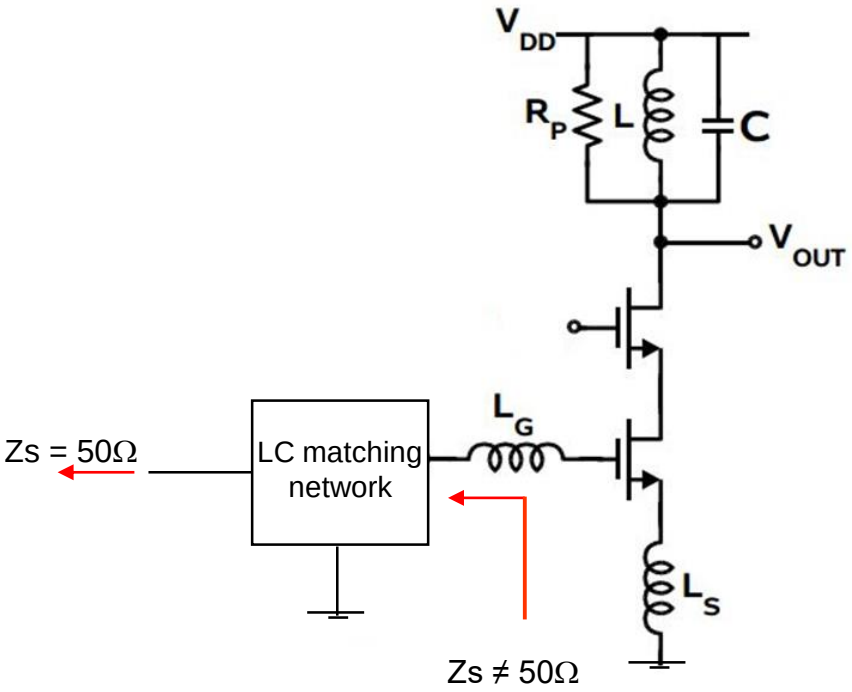
LNA with wide range of gain steps and linearity:



Sam Tan et. al, JSSC 2012

- Sometimes it is hard to implement all gain range in a single LNA stage
- A dual-path LNA sometimes is used to implement a wide range of LNA gain control

Manipulating Rs to different value via matching to improve LNA

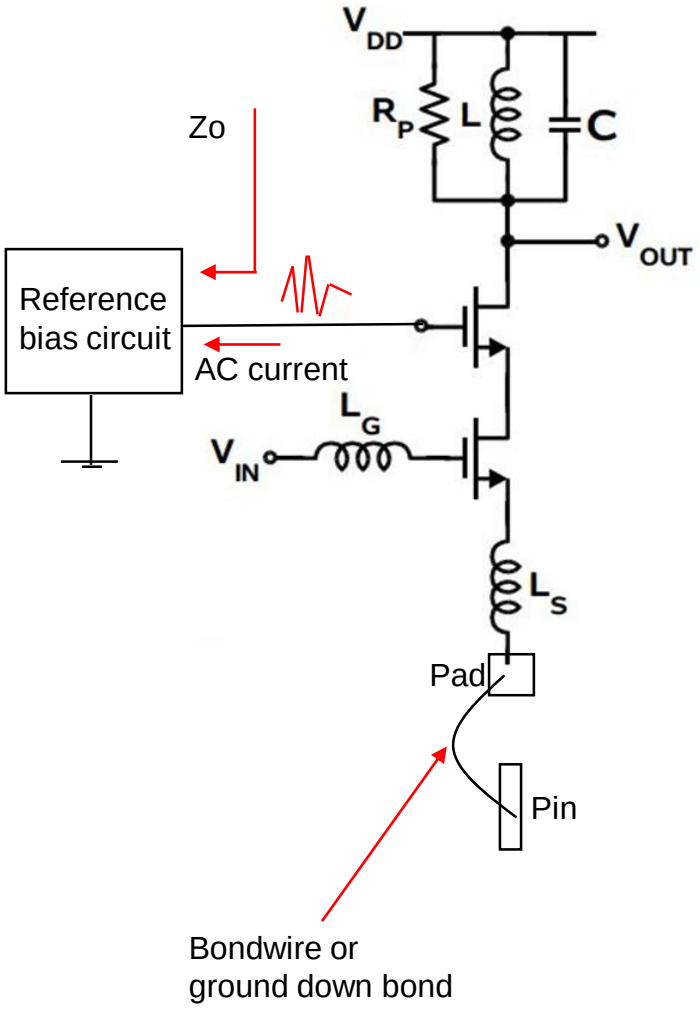


- Sometimes shifting the 50Ω source impedance to a higher/lower value can be better for LNA design (reduced device size for lower power, reduced Ls, etc.) via passive LC matching network
- The matching network can also provide voltage gain, which improved cascaded receiver gain and Rx NF
- In reality, however, finite Q of matching network elements (especially inductors) can significantly degrade NFmin (and so NF) of LNA

What about the cascode bypass?

The circuit generating the proper bias voltage for the cascode device has a finite output impedance. The AC gate current of the cascode device results in a finite AC swing at the base of the cascode. This can result in increased distortion in the LNA. Moreover the noise from the cascode bias circuit can become significant.

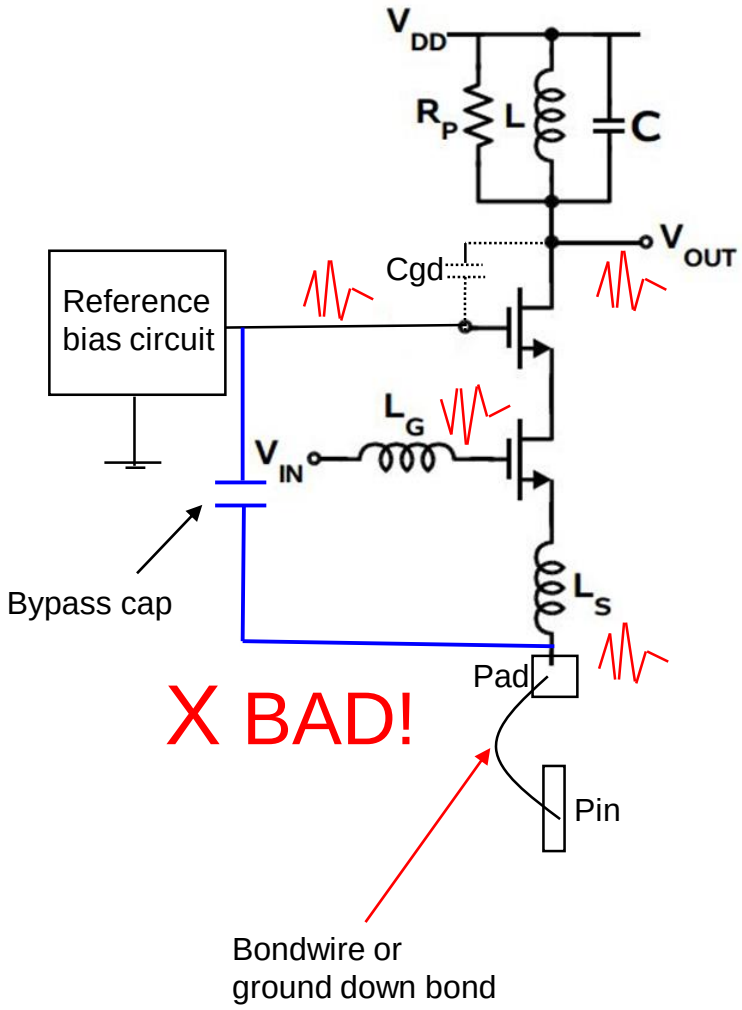
To overcome this problem, a large bypass capacitor needs to be connected from the cascode gate to a separate ground. Note that if this cap shares the LNA core ground by mistake, a potential instability occurs.



Separating LNA core ground from cascode bypass ground:

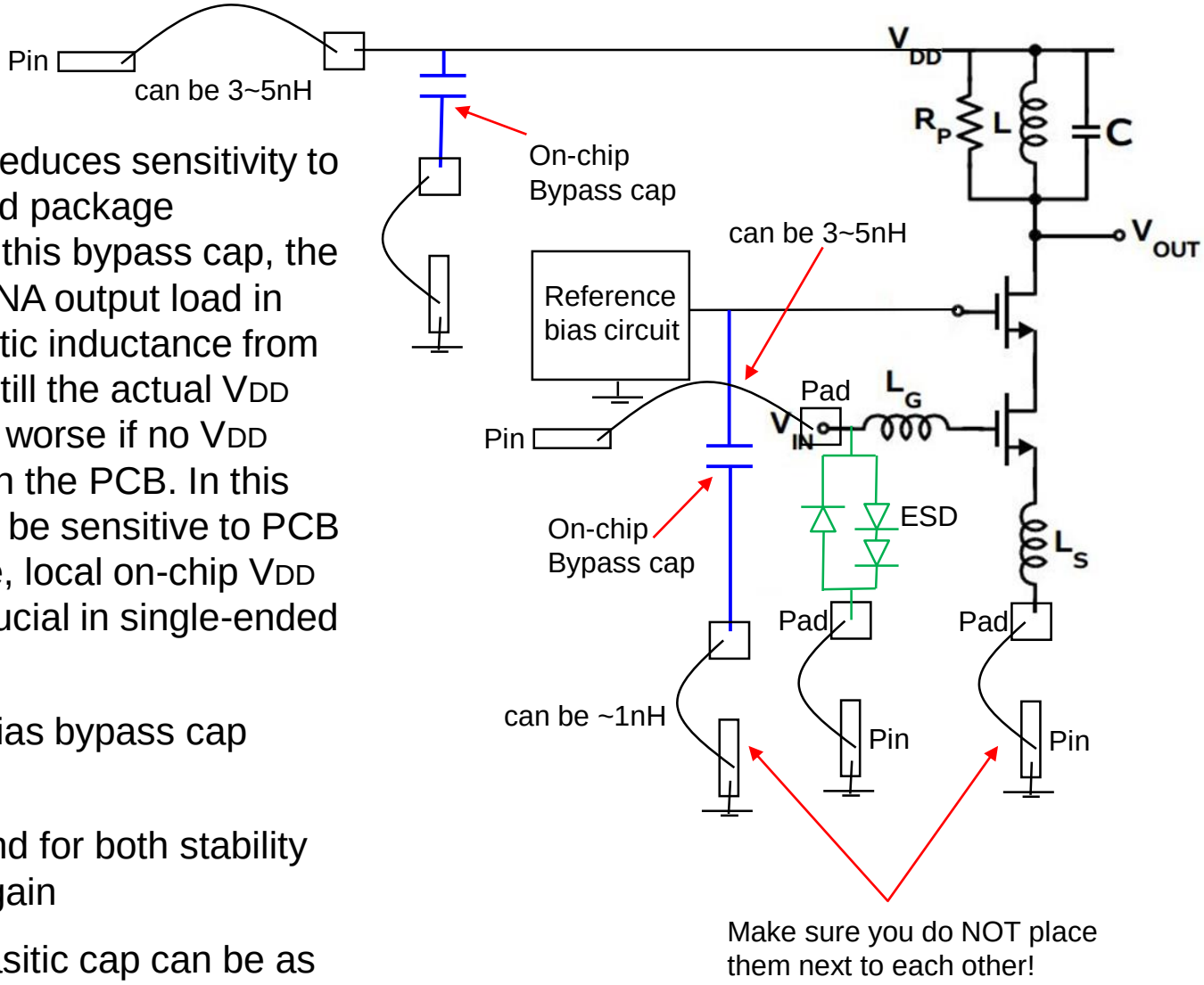
The output swing couples through Cgd of the cascode device to its gate. The bypass cap then couples this swing to the ground pad. Because of the finite impedance at the ground pad caused by the finite ground inductance, the LNA ground would bounce with opposite phase compared to the RF input. The loop then is a positive feedback and can result in LNA instability.

It is therefore important to ground the bypass can to a separate ground from the LNA core.

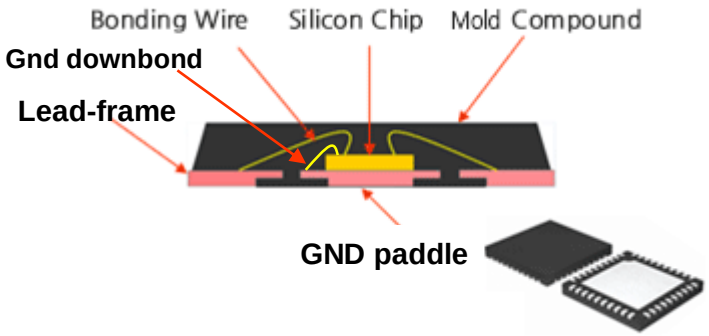


Single-ended LNA complete picture:

- V_{DD} supply bypass reduces sensitivity to V_{DD} line parasitic and package inductance. Without this bypass cap, the output will see the LNA output load in series with all parasitic inductance from LNA local V_{DD} node till the actual V_{DD} pin. The matter gets worse if no V_{DD} bypassing is done on the PCB. In this case, the design will be sensitive to PCB parasitics. Therefore, local on-chip V_{DD} bypassing is very crucial in single-ended LNA design.
- Separate cascode bias bypass cap ground for stability
- Separate ESD ground for both stability and less impact on gain
- Input pad+ESD parasitic cap can be as large as 100fF.

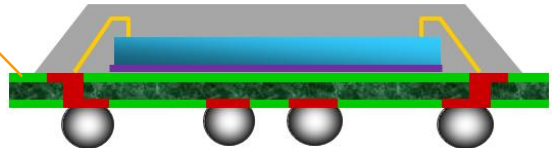


Different types of RF packages:

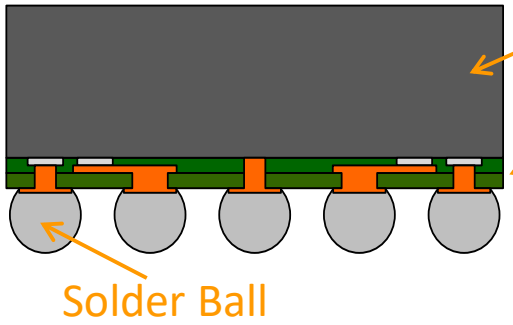


QFN PKG

Substrate



Wire-bond Ball Grid Array (WB-BGA)

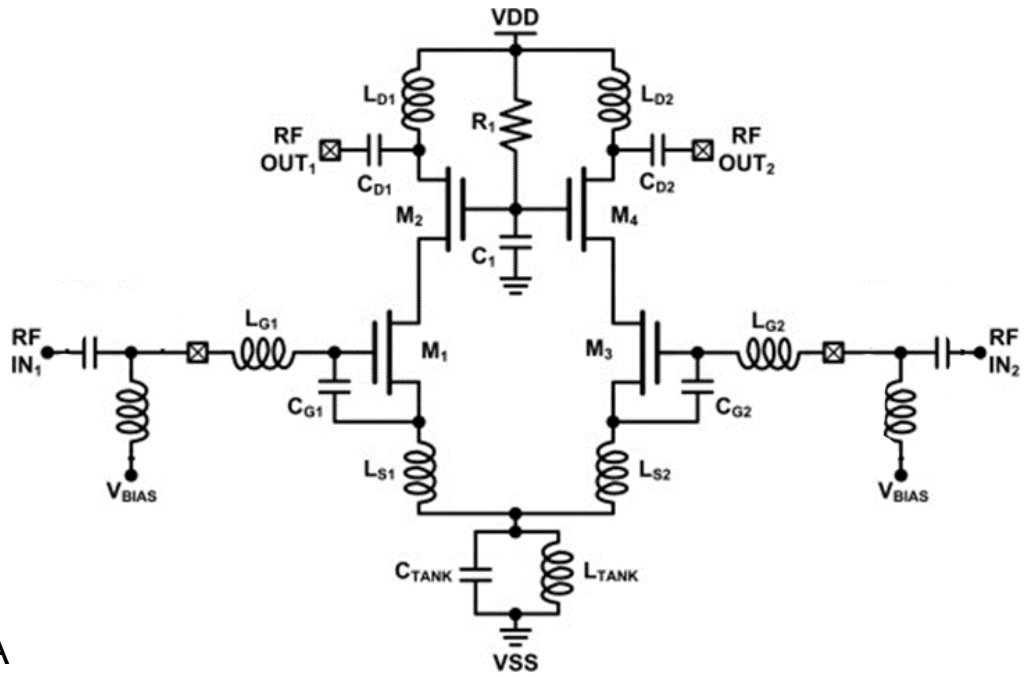


Wafer-level chip-scale package (WLCSP)

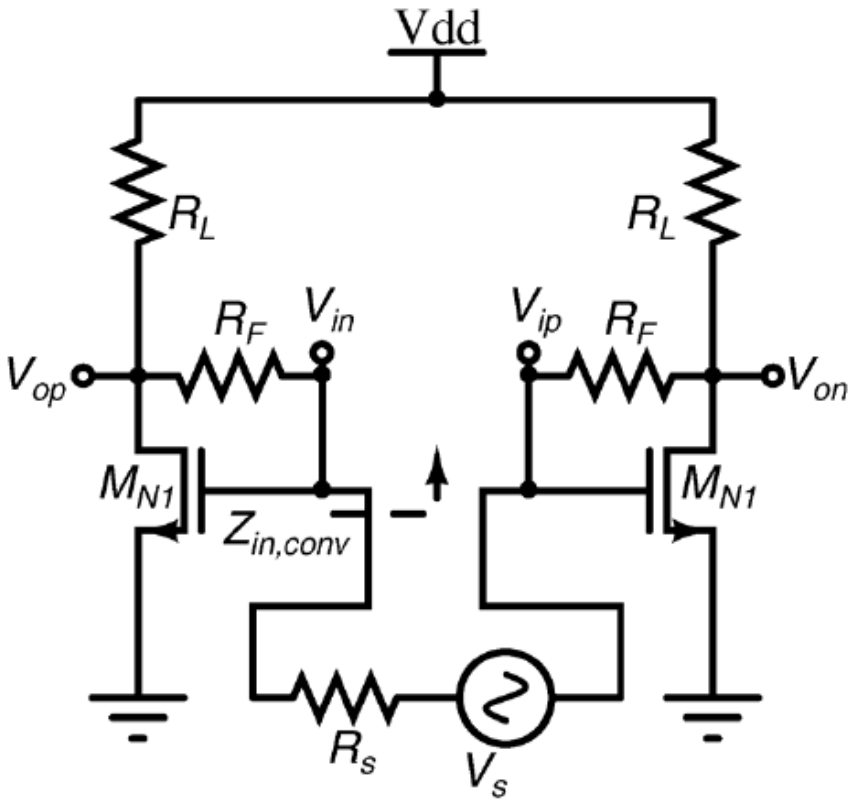
- QFN package is the cheapest package but has largest footprint
- BGA is usually used for large number I/O SoC for smaller PCB area than QFN
- WLCSP provides the lowest area and has lowest package parasitics

Differential LNA:

- less sensitive to V_{DD}, ground, package and cascode bias parasitic inductance
- insensitive to some common mode noise (substrate, supply, etc.), but still can be sensitive to bias noise desense
- needs a balun to interface with duplexer or antenna (big disadvantage)
- double the area of single-ended LNA
- usually double the power of single-ended LNA
- Need to check both differential AND common-mode stability!
- Can be designed to provide almost same NF as single-ended LNA!



broadband LNA: conventional

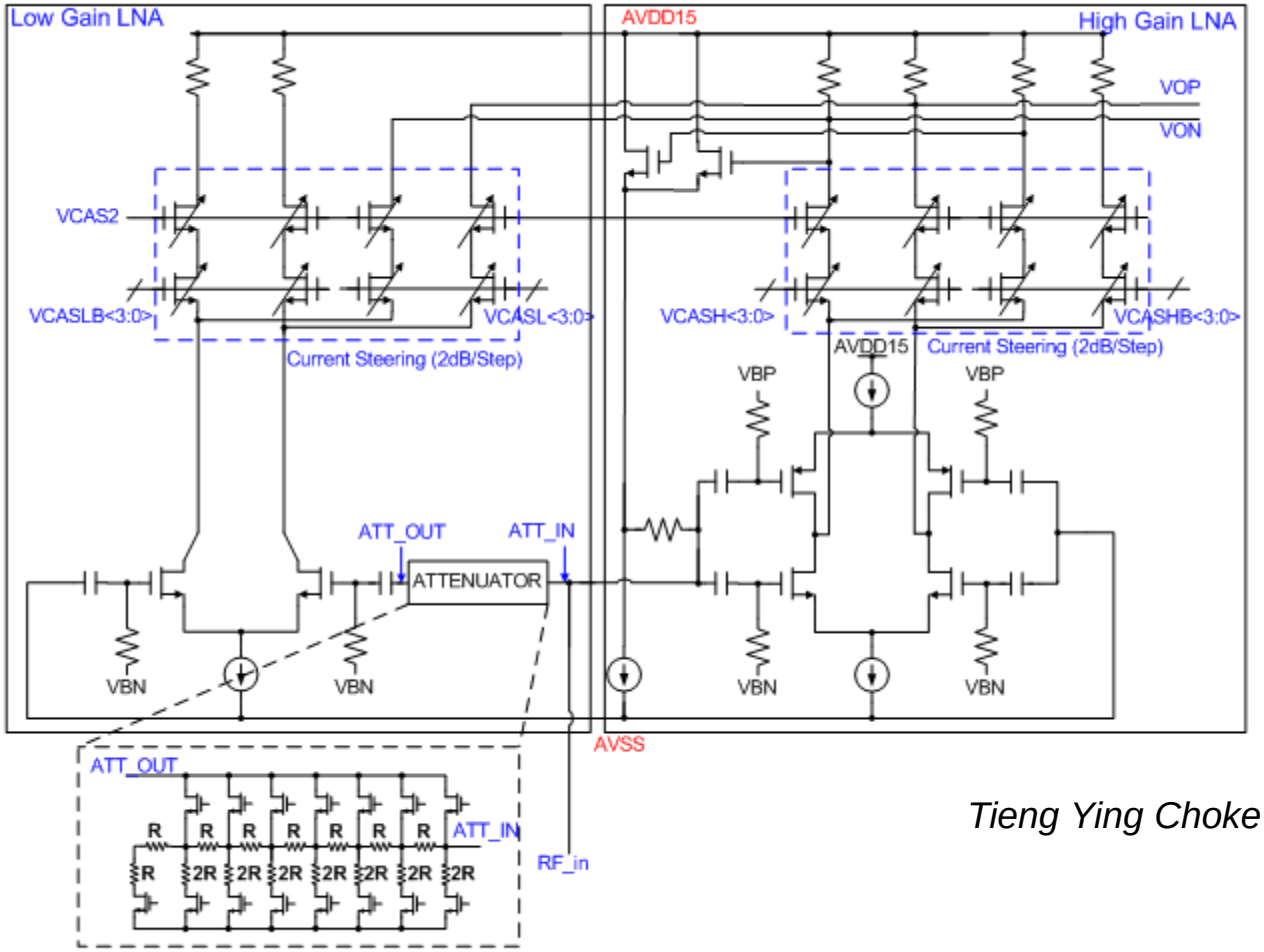


El-Nozahi et. Al, JSSC 2011

$$\mathrm{NF}_{conv} = 1 + \frac{2\gamma_n}{g_{m,n}R_s} + \frac{1}{2}\left(1 + \frac{2}{g_{m,n}R_s}\right)^2 \frac{R_s}{R_F} + \frac{2}{g_{m,n}^2 R_L R_s}.$$

- Achieves both input and output match by proper choice of RF, RL and gm
- To improve NF, need to increase gm, increase RF and RL
- For a given gain, noise is usually dominated by transistor and feedback resistor RF

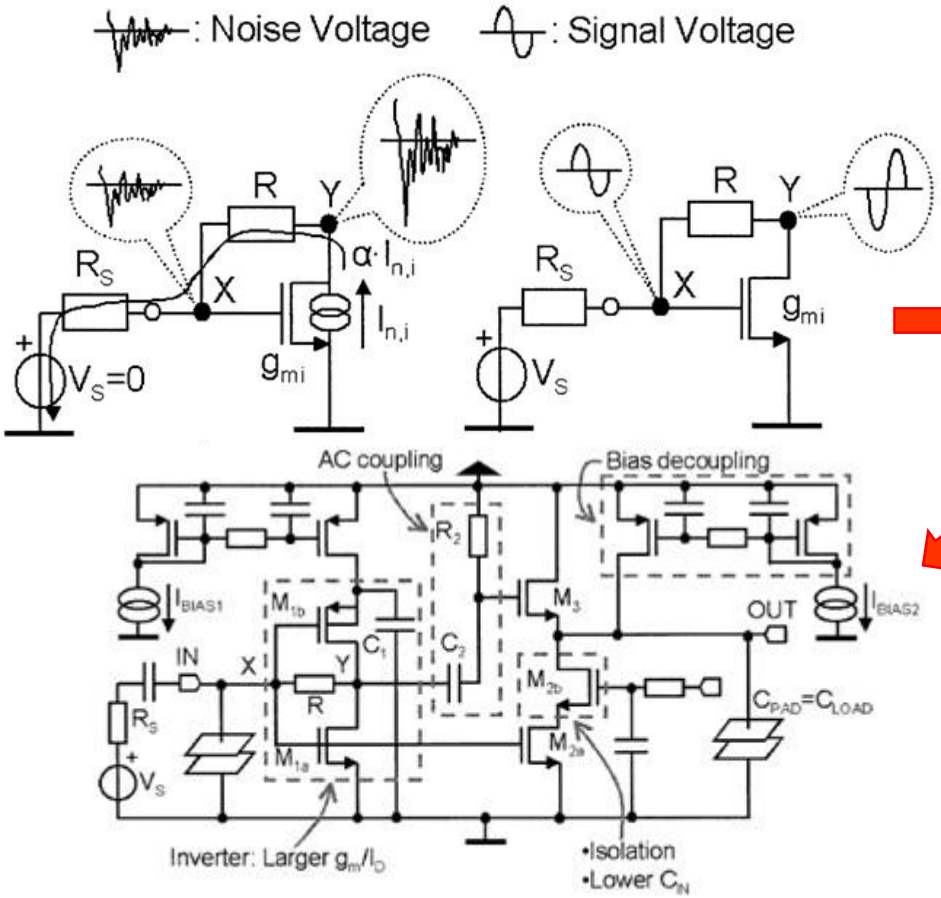
broadband LNA: conventional (TV-tuner LNA, complete)

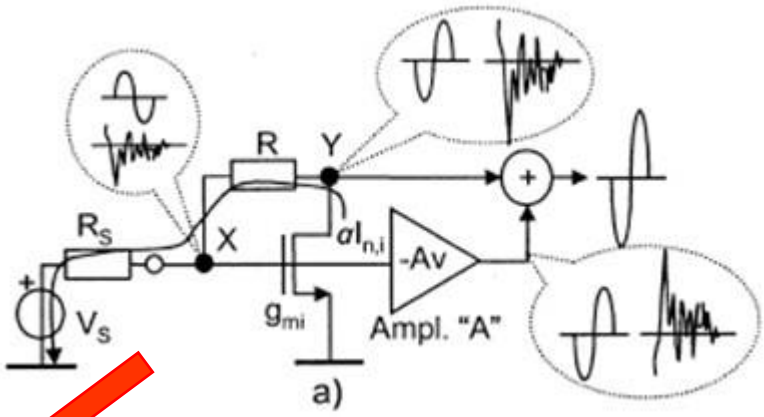


Tieng Ying Choke et. Al, JSSC 2013

- Source follower isolated RL from RF
- Current-steering for gain control
- Low-gain path with attenuator at input for further gain control

broadband LNA: noise cancelling





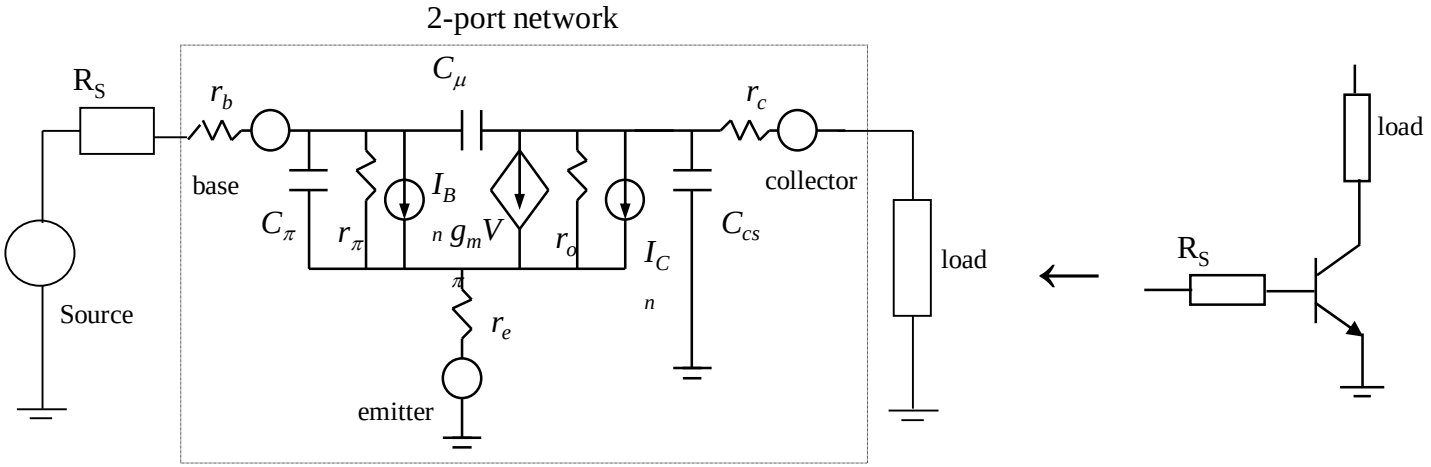
F. Bruccoleri et. al, ISSCC 2002

- Cancels first-stage amplifier thermal noise
- Works well over PVT
- Noise from canceling circuit overhead

Appendix: Bipolar LNA Design

- **BJT Low noise amplifier**
  - Minimum vs. optimum NF of a BJT
  - Simultaneous power and NF match
  - LNA design example
  - Design for linearity and design for low power

Noise equations for a CE bipolar transistor:



The figure shows the small-signal noise model of a bipolar transistor, where I_{Cn} and I_{Bn} represent the shot noise current associated with the collector and base DC currents, respectively. In order to apply the *NF* analysis derived to the circuit above, the transistor has to be treated as a 2-port network and all its internal noise sources are then represented by equivalent two noise sources at the input (V_n and I_n).

Applying small-signal circuit analysis results in having an equivalent input noise sources of:

$$\overline{V_n^2} = 4kT\Delta f\left[(r_b + r_e) + \frac{V_T}{2I_C}\right] \quad \text{and} \quad \overline{I_n^2} = 2q\Delta f\,\frac{I_C}{\beta_{DC}}\left(1 + \frac{1}{\beta_{DC}}\left(1 + \frac{\beta_{DC}^2 f^2}{f_T^2}\right)\right)$$

The current practice by designers to lower the device noise is to lower V_n. This is commonly done: (i) by using the largest possible device to lower (*rb* + *re*), and (ii) by using the maximum available current to increase g_m. This technique leads to a non-optimum design because it ignores the equivalent input noise current, I_n, and its partial correlation with the equivalent input noise voltage source, V_n. Increasing the device size indefinitely for a given collector current results in lowering the f_T causing the input noise current I_n in to increase. Similarly, the continuous increase of the bias current for a given device size results in reduction in the current gain β_{DC} forcing the input noise current I_n to increase degrading the *NF*. A systematic analytical design method needs to be developed to address these problems and lead to an absolute optimum design for LNAs. We will focus on the LNA *NF* because it determines the overall front-end sensitivity. In order to achieve minimum *NF*, the LNA should be matched to its optimum noise figure source impedance, which in general will not equal 50 Ω

Fukui showed, with cumbersome math applying the 2-port noise theory to BJT in CE configuration, that the minimum achievable *NF* for a bipolar device in a common-emitter configuration is

$$NF_{\min} = 1 + \frac{n}{\beta_{DC}} + \sqrt{\frac{2I_C}{V_T}(r_e + r_b)\left(\frac{f^2}{f_T^2} + \frac{1}{\beta_{DC}}\right) + \frac{n^2}{\beta_{DC}}}$$

where n is the junction grading factor ranging from 1 to 1.2. Almost all parameters, except for V_T, are bias dependent; i.e. they are a function of I_C. It is useful to plot NF_{min} vs. collector current taking very carefully the bias dependencies into account.

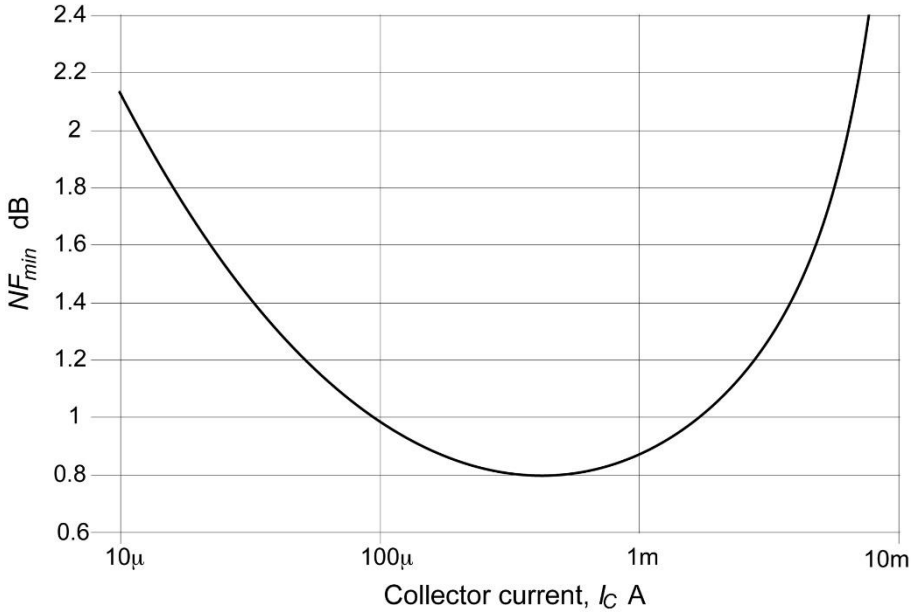


Fig. 4.3

Although each point on Fig. 4.3 is called NF_{min}, Fig. 4.3 shows that the NF_{min} (I_C) has an absolute minima. We will call this the optimum *NF* point, NF_{opt}, at which the device has to operate for best noise figure performance. The plot of Fig. 4.3 is repeated for various bipolar devices in the same technology with various geometry as seen in Fig. 4.4 which shows that all devices have almost the same NF_{opt} but at different bias currents depending on the size of the device.

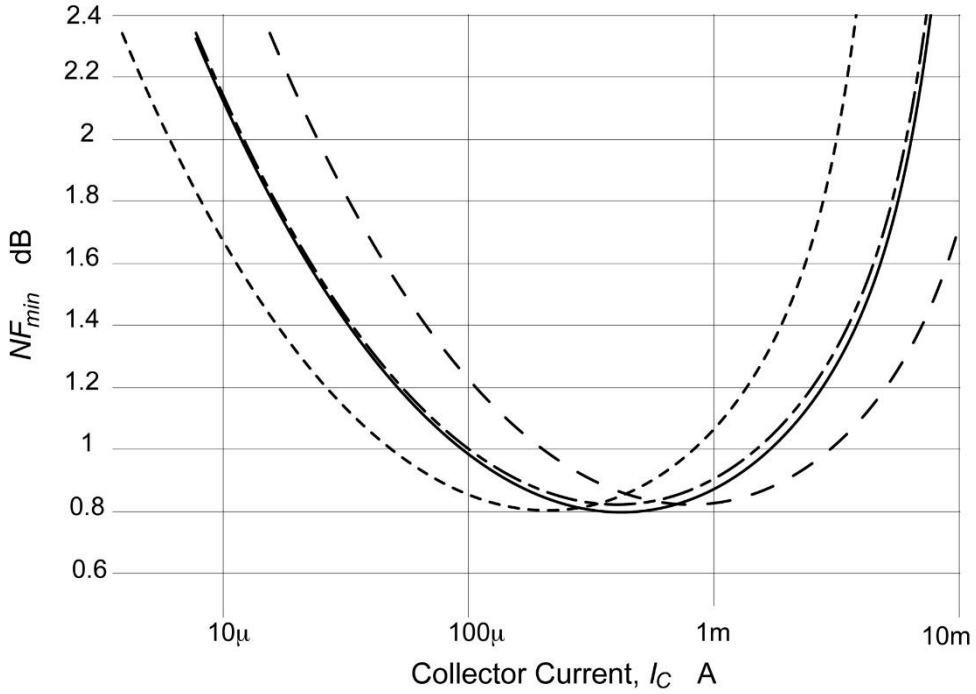


Fig. 4.4

By plotting the NF_{min} vs. collector current density, all devices show to have the same NF_{opt}, within a tenth of a dB, occurring at the same collector current density as shown in Fig. 4.5. This means that the achievable NF_{opt} is almost independent of the choice of the device geometry for a given bipolar technology. The designer basically can pick any geometry, for it has little effect on the achieved *NF*. To this stage, only the optimum bias current density has been calculated. The proper device sizing and the resulting bias current will be addressed next.

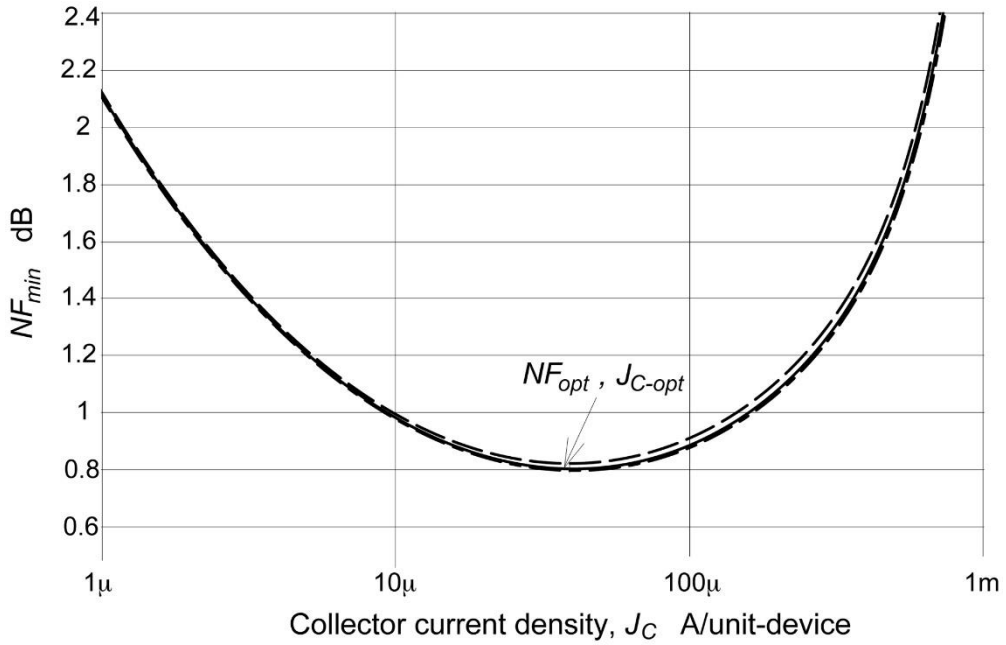


Fig. 4.5

The optimum source impedance at the NF_{opt} point is unlikely to equal the source impedance. This impedance mismatch typically creates a tradeoff between optimizing power match and *NF*. For optimum power match, an LNA has to be matched to the driving source impedance which is typically 50 Ω. For optimum *NF*, on the other hand, the LNA has to be matched to $R_{S\text{-}opt}$ instead. Fukui, however, showed an expression for the optimum source resistance to achieve NF_{min} of a bipolar device in a common-emitter configuration given by.

$$R_{S-opt} \cong \frac{f_T}{f}\left(\frac{n^2 V_T}{2I_C} + (r_e + r_b)\right)\left(\frac{\sqrt{\frac{I_C}{2V_T}(r_e + r_b)\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right) + \frac{n^2 f_T^2}{4\beta_{DC} f^2}}}{\frac{I_C}{2V_T}(r_e + r_b)\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right) + \frac{n^2}{4}\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right)}\right)$$

Any device with a certain geometry has its own size *N* relative to the unit-device. A unit- device is the minimum size transistor in a given bipolar technology. Therefore $R_{S\text{-}opt}$ can be rewritten for any device with any given geometry as a function of its relative size *N* and the current density, *JC*, as

$$R_{S-opt} \cong \left(\frac{1}{N}\right)\left\{\frac{f_T}{f}\left(\frac{n^2 V_T}{2J_C} + (r_e + r_b)_u\right)\left(\frac{\sqrt{\frac{J_C}{2V_T}(r_e + r_b)_u\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right) + \frac{n^2 f_T^2}{4\beta_{DC} f^2}}}{\frac{J_C}{2V_T}(r_e + r_b)_u\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right) + \frac{n^2}{4}\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right)}\right)\right\}$$

where $(r_b + r_e)_u$ is for a unit-device. If M devices of the same geometry are used in parallel to increase the overall device size, $R_{S\text{-}opt}$ can be rewritten as a function of collector current density, J_C, and device size M as,

$$R_{S-opt}(M) \cong \left(\frac{1}{MN}\right)\underbrace{\left\{\frac{f_T}{f}\left(\frac{n^2 V_T}{2J_C} + (r_e + r_b)_u\right)\left(\frac{\sqrt{\frac{J_C}{2V_T}(r_e + r_b)_u\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right) + \frac{n^2 f_T^2}{4\beta_{DC} f^2}}}{\frac{J_C}{2V_T}(r_e + r_b)_u\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right) + \frac{n^2}{4}\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right)}\right)\right\}}_{\text{Constant for fixed } J_C}$$

$R_{S\text{-}opt}$ varies as M varies. In fact, $R_{S\text{-}opt}$ is inversely proportional to M. This means that by selecting the device size properly, it is possible to set $R_{S\text{-}opt} = R_S$, which could be 50 Ω for example. The illustrated procedure simultaneously achieves maximum power transfer and minimum *NF* for the common-emitter stage with the same matching network. The objective now is to find the device size, M, that sets $R_{S\text{-}opt}$ = 50 Ω while keeping the device operating at the NF_{opt} point. In order not to disturb the value of the NF_{opt} while varying M, the optimum device collector current density, $J_{C\text{-}opt}$, should be held constant. For each value of M, the parameters in the $R_{S\text{-}opt}$ are extracted to calculate the corresponding $R_{S\text{-}opt}$ value, which is plotted as a function of M and $1/M$ as shown next (f = 1.8 GHz).

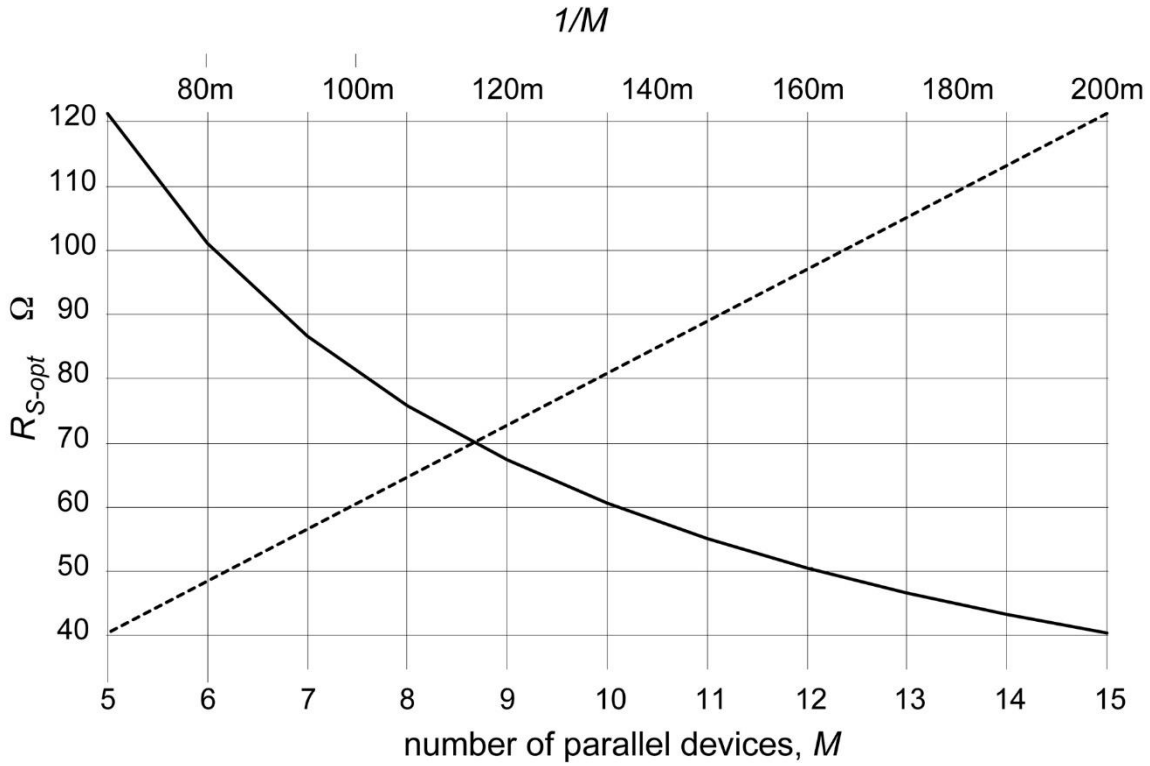


Fig. 4.6

It can be seen from Fig. 4.6 that $R_{S\text{-}opt}$ equals 50 Ω at some *M* value depending on the geometry of the selected bipolar device and its relative size *N* compared to the unit-device. Note that the product *MN* gives the final device size relative to the unit-device. Once the final device size has been determined (*MN*), the total required bias current will be determined as

ICC* = optimum current density $J_{C\text{-}opt}$ × chosen device size *N* relative to the unit–device × number of devices in parallel *M

A 1.8 GHz LNA Design Example:

This design example is based on the cascode topology whose *NF* is dominated by the common-emitter input device. A simplified schematic is shown in Fig. 4.7. The technology picked for this example is a 30 GHz SiGe bipolar. Since the LNA *NF* is dominated by the common-emitter input device, Q1, the optimization procedure discussed in lecture is followed to select the optimum size and bias current for Q1.

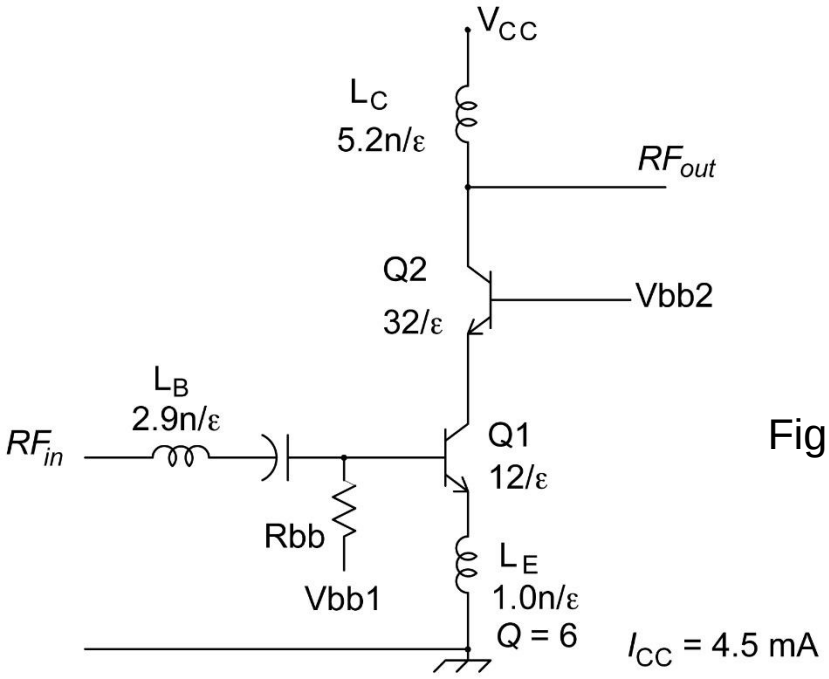


Fig. 4.7

The minimum *NF* vs. current density function has been calculated (using Spectre RF) for this technology similar to the graph in Fig. 4.5. The NF_{opt} was found to be 0.8 dB at a current density of 38 μA/unit-device for an operating frequency of 1.8 GHz. Since the device geometry has insignificant effect on the value of NF_{opt}, we picked a device of three base and two emitter contacts. This device has a relative size *N* of 10 times the unit-device, therefore, the input device Q1 is biased at a current density of 380 μA/device to operate at the NF_{opt} point for f = 1.8 GHz. In order to set $R_{S\text{-}opt}$ of the input device Q1 to 50 Ω (see Fig. 4.6), twelve of these devices are used in parallel (M = 12). As a result, the total bias current is set to be 380 μA/device ×12 devices ≈ 4.5 mA.

An on-chip spiral inductor L_E, with a Q of 6 at 1.8 GHz, is used to match the LNA input to a 50 Ω source while an off-chip inductor L_B resonates with the reactance of the input impedance. For the common emitter device, Q1, with inductive degeneration, the value of L_E and L_B can be expressed as

$$L_E = \frac{50\,\Omega}{2\pi f_T} \qquad \text{and} \qquad L_B = \frac{1}{(2\pi f)^2 C_{\pi 1}} - L_E$$

where $C_{\pi 1}$ is the total base-emitter capacitance of Q1. Note that the addition of L_E and L_B ideally does not affect the value of $R_{S\text{-}opt}$.

The calculated noise figure of the LNA as well as the theoretical NF_{min}, assuming an $R_{S\text{-}opt}$ match, are plotted vs. frequency as shown in Fig. 4.8. It can be seen from Fig. 4.8 that the two plots touch with a value of 1.1 dB at the frequency of interest of 1.8 GHz, indicating that $R_{S\text{-}opt} = R_S = 50\ \Omega$ at that frequency. Trying to increase or decrease the bias current beyond 4.5 mA causes the *NF* to increase, indicating that the LNA is indeed operating at the NF_{opt} point.

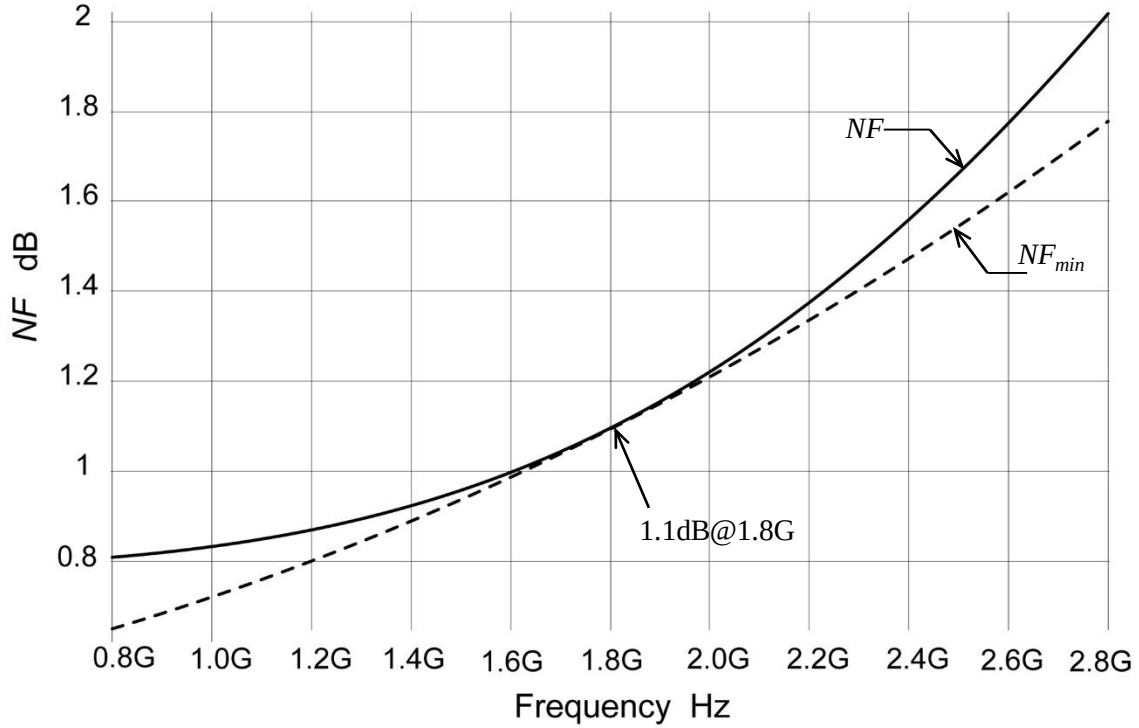


Fig. 4.8

Frequency-Scalable LNA Design:

$$NF_{\min}(J_C) = 1 + \frac{n}{\beta_{DC}} + \sqrt{\frac{2J_C}{V_T}(r_e + r_b)_u\left(\frac{f^2}{f_T^2} + \frac{1}{\beta_{DC}}\right) + \frac{n^2}{\beta_{DC}}}$$

The f_T for a bipolar device can be expressed as

$$f_T^{-1}(J_C) = 2\pi\left(\tau_F + \frac{C_{je} + C_{jc}}{g_m}\right) = 2\pi\left(\tau_F + V_T\frac{(C_{je} + C_{jc})_u}{J_C}\right)$$

where τ_F is the base transit time, and $(C_{je} + C_{jc})_u$ are the base-emitter and base-collector junction capacitance for a unit-device, respectively. Substituting the f_T in the NF_{min} equation yields

$$NF_{\min} = 1 + \frac{n}{\beta_{DC}} + \sqrt{aJ_C + b + \frac{c}{J_C}}$$

where the parameters *a*, *b*, and *c* are

$$a = \frac{2}{V_T}(r_b + r_e)_u\left(4\pi^2\tau_F^2 f^2 + \frac{1}{\beta_{DC}}\right) \qquad b = 16\pi^2\tau_F(r_b + r_e)_u(C_{je} + C_{jc})_u f^2 + \frac{n^2}{\beta_{DC}}$$

$$c = 8\pi^2 V_T(r_b + r_e)_u(C_{je} + C_{jc})_u^2 f^2$$

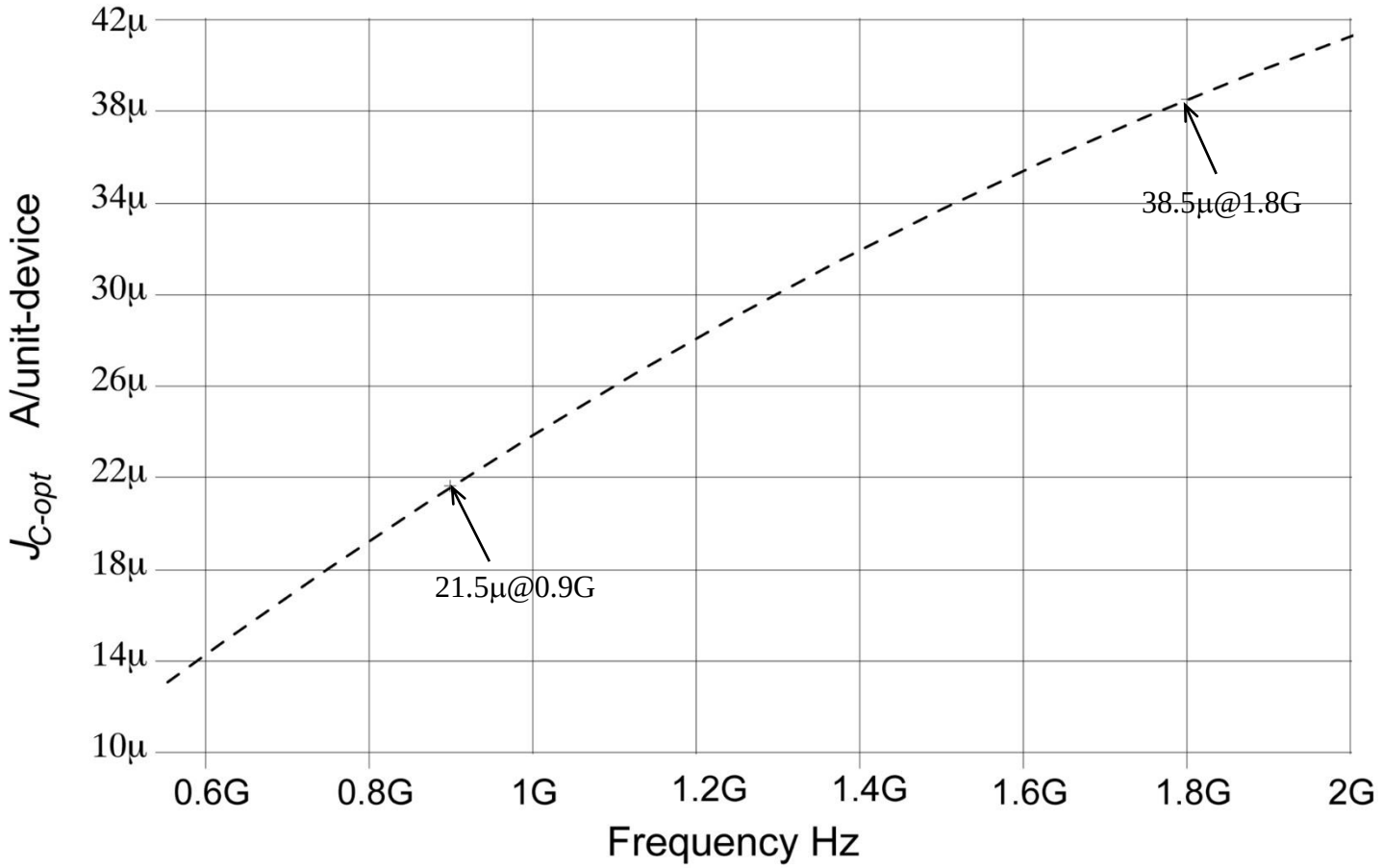
To simplify the analysis, β_{DC}, r_b, r_e, C_{je}, C_{jc}, and n are assumed to be constant as a function of collector current density. This is valid since the base resistance at such current densities varies very little with collector current. Same is true for the parasitic junction capacitance and the junction grading factor n. Also the change in β_{DC} is less than 5 percent when the device is biased considerably below its peak f_T. Taking the first derivative of NF_{min} with respect to collector current density, J_C, yields

$$\frac{\partial NF_{\min}}{\partial J_C} = \frac{a - \frac{c}{J_C^2}}{2\sqrt{aJ_C + b + \frac{c}{J_C}}} = 0$$

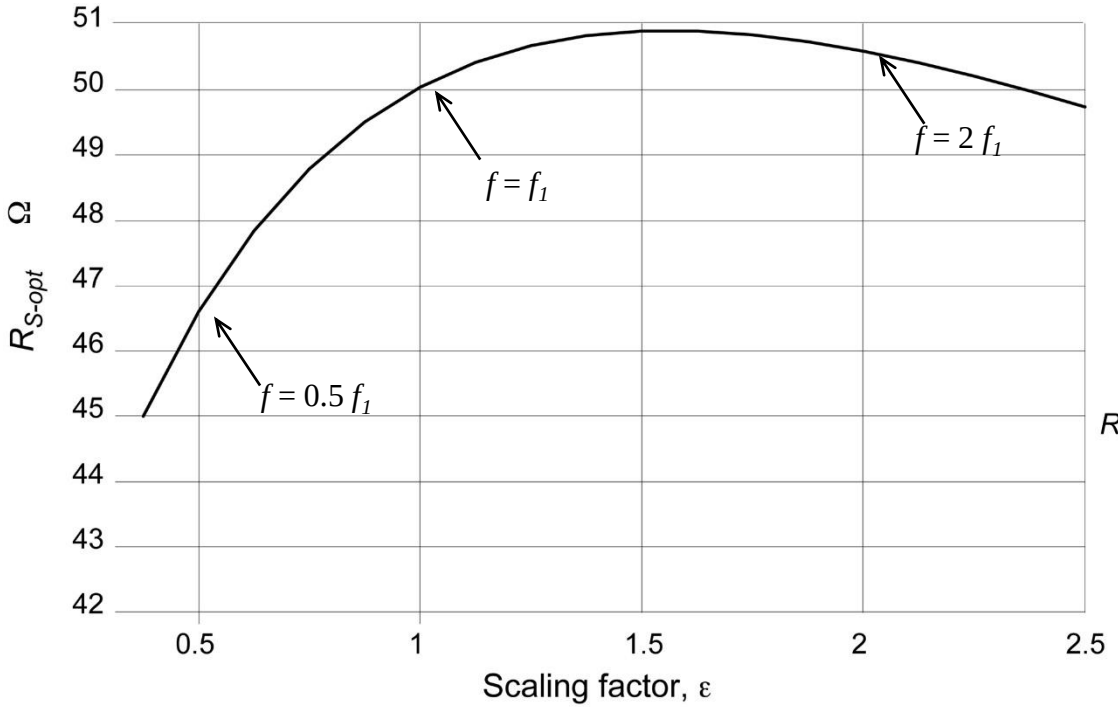
$$J_{C-opt} = \sqrt{\frac{c}{a}} = 2\pi(C_{je} + C_{jc})_u V_T \sqrt{\frac{\beta_{DC} f^2}{4\pi^2 \beta_{DC} \tau_F^2 f^2 + 1}}$$

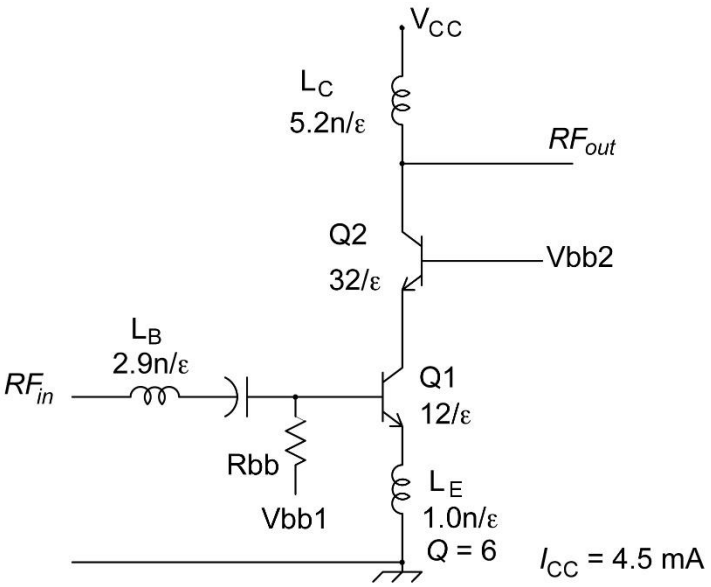
For frequencies well below f_T, $J_{C\text{-}opt}$ scales almost linearly with frequency, which means that the optimum collector current density scales by the same factor as the operating frequency. For frequencies well below f_T, the term becomes <<1, therefore $J_{C\text{-}opt}$ in this case can be approximated to be

$$J_{C-opt} \approx 2\pi(C_{je} + C_{jc})_u V_T \sqrt{\beta_{DC}} f$$



Therefore, one would start with say 900MHz LNA, and by mere scaling of LNA elements by a factor of 0.5 (keeping same bias current) a 1.8GHz LNA is obtained!

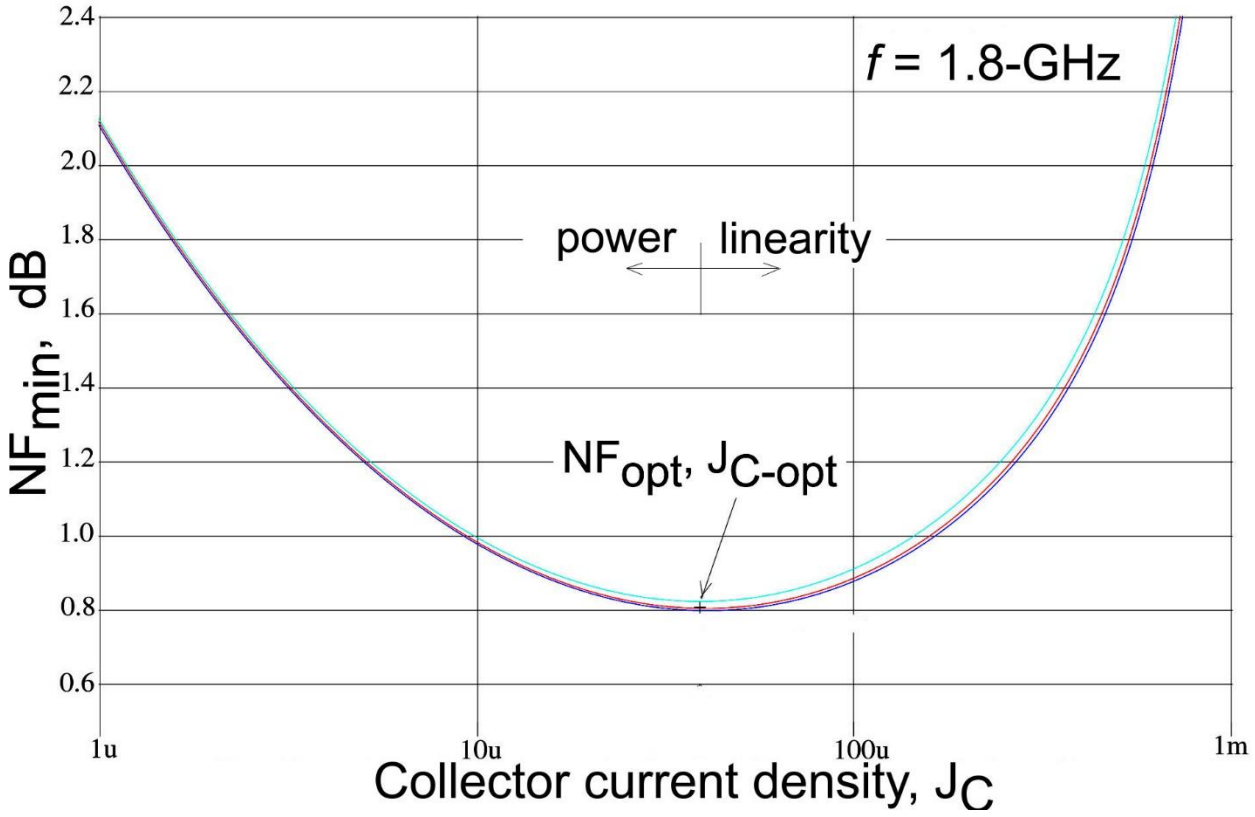




Note that Rs-opt varies little with the proposed device scaling method. The LNA circuit scale with frequency via the frequency scaling factor ε keeping the total current the same.

LNA Design Under Power-Constraint

In some wireless applications, the DC power consumption of the LNA is a primary concern. Such systems can tolerate a small degradation in noise figure if that achieves a large savings in the LNA power consumption.



Find $J_{C\text{-}opt}$

⇩

Sweep device size to set $R_{S\text{-}opt}$

⇩

Set power consumption

Find J_C and so NF_{min}

⇧

Sweep device size to set $R_{S\text{-}opt}$

⇧

Set power consumption

we start first with the bias current dictated by the power consumption constraint, then the device size is varied to set the optimum source resistance to equal the source impedance keeping the total bias current fixed. As a result, the current density is set and so the achievable *NF* (Fig. 4.9). In this case, the device will operate at one of the NF_{min} points to the left of the NF_{opt} point, depending on the obtained current density. This procedure guarantees that the designer will obtain the minimum *NF* out of an LNA given a certain power consumption. Using this technique, a 900 MHz LNA has been designed, given a power consumption of 2 mW (VCC = 2.7 V). The achieved *NF* was 1.4 dB with a power gain of 13 dB.

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