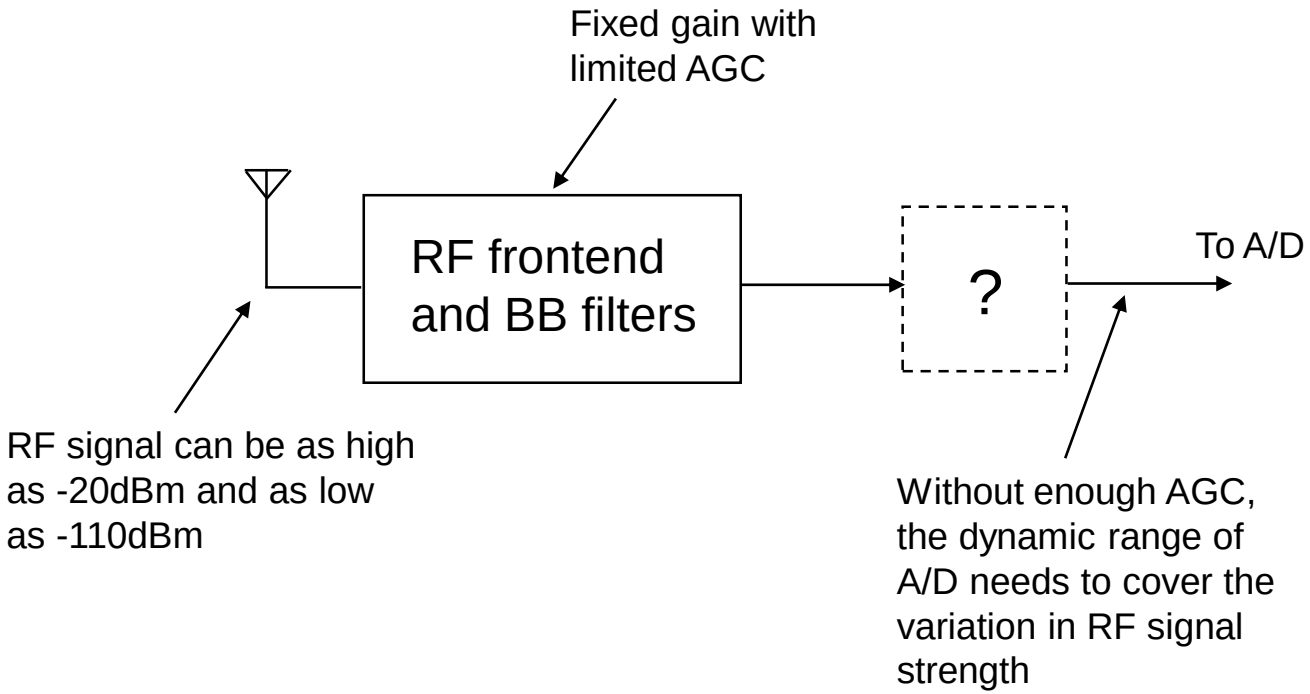
Variable-gain amplifier design (VGA)
a.k.a
Programmable-gain amplifier (PGA)

- **VGA/PGA design**
  - why a VGA/PGA is needed?
  - Important VGA/PGA specs
  - Commonly used VGA/PGA topologies
  - Linear dB/V AGC control
- **References**

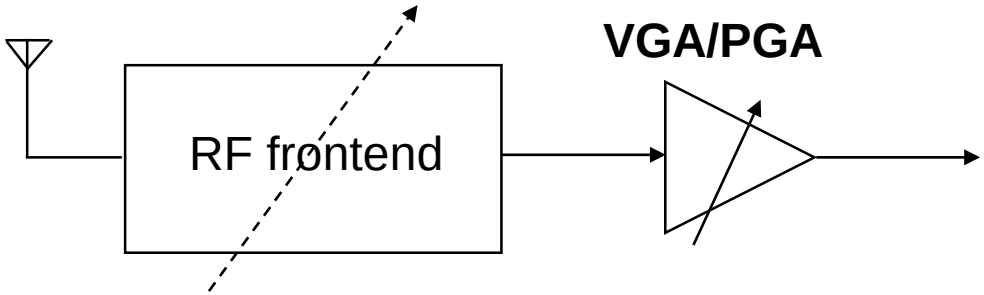
Why a VGA/PGA is needed in a receiver?



• on-chip AGC relaxes the required A/D dynamic range. AGC budget is usually split between RF frontend and baseband with the bulk being at baseband (with finer steps) since it is easier to implement.

Important VGA/PGA specs:

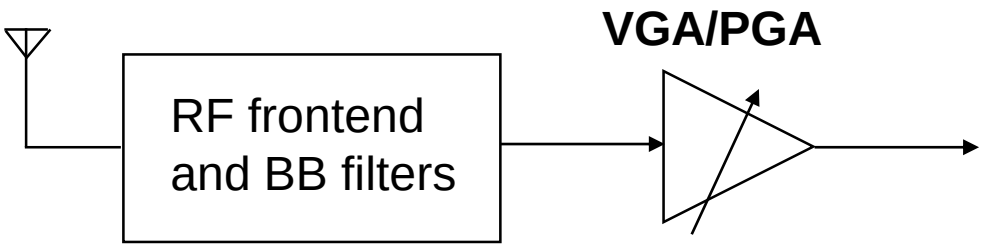
1. AGC range:



The AGC range is calculated based on the range of the receive signal strength at the antenna. If the RF fronend carries no AGC, then the AGC is made all at the VGA/PGA. Note that a margin needs to be added to cover variation over PVT.

For example, if the desired RF signal varies from -110dBm to -30dBm, then the required AGC range is 80dB. To add margin the AGC range is extended to 90dB, to cover variation of front-end gain over PVT. If the RF frontend has 30dB of AGC, then the VGA needs to have 60dB of AGC.

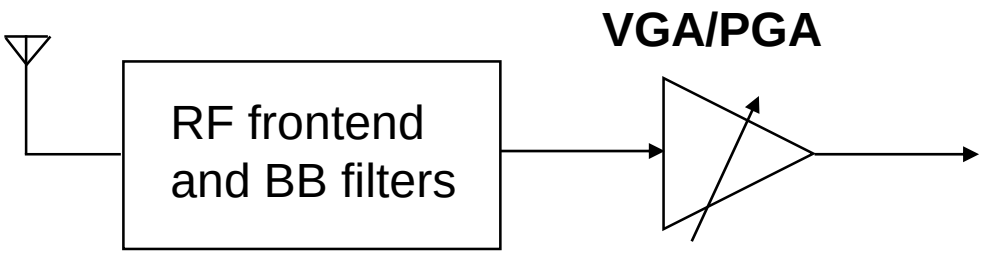
2. Maximum and minimum VGA/PGA gain:



The max gain is calculated based on the minimum RF signal level and the desired swing at the A/D input, given a certain RF frontend gain. The min gain is calculated based on the maximum RF signal level and the desired swing at the A/D input given a certain RF frontend gain.

For example, the desired swing at the A/D input (Set point) is 0dBm, and the max and min RF signal are -30dBm and -110dBm, respectively. Let us also assume that the max RF frontend gain is 40dB with 30dB of AGC set in the RF frontend. This means the max VGA gain needs to be 110-0-40=70dB. The min VGA gain is then 0-(-30+40-30)=20dB. The min gain can also be calculated from the AGC range as 110-30=80dB. With 30dB AGC in frontend, the VGA needs to have 50dB of AGC. With VGA having 70dB of max gain, the min gain is then 70-50=20dB.

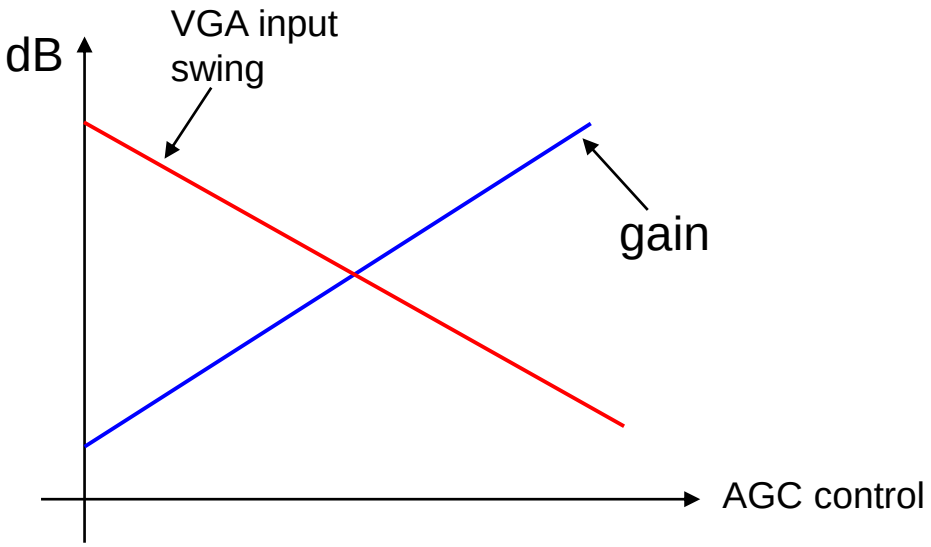
3. Input referred noise:



$$F = 1 + F_{LNA} + ... + \frac{0.5F_{VGA}}{G_{frontend} - 1}$$

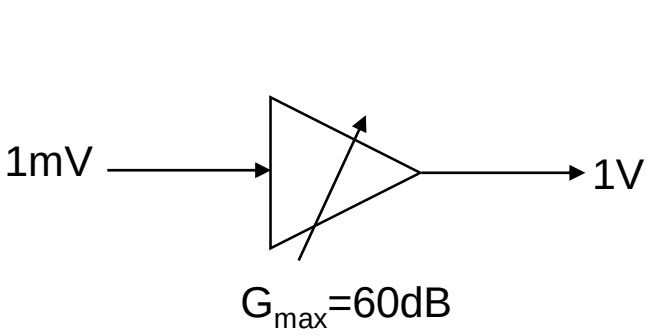
For direct conversion receivers, there is not much gain ahead of the VGA and so its noise then becomes important at sensitivity. The max input referred noise of the VGA at max gain is calculated based on the noise budget allowed for the VGA and the desired overall receiver NF.

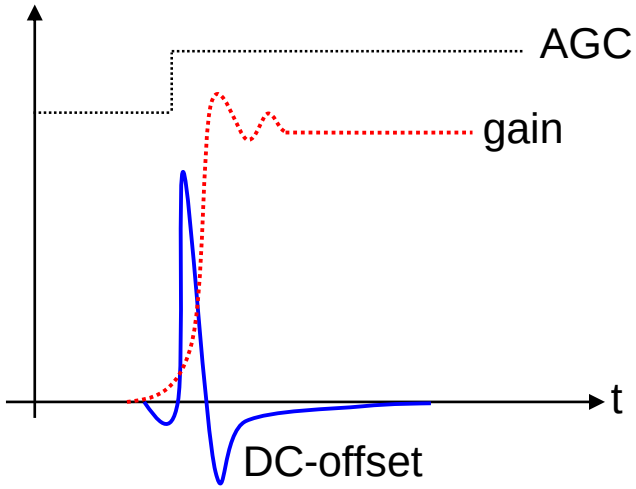
4. compression:



From the graph above, it is clear that the input referred compression is most difficult at minimum VGA gain since the signal swing at the input is at its max. A good VGA topology is that whose input compression increases as VGA gain decreases. VGA compression is usually set to be 6dB above the max signal peak swing at the input/output. VGA output compression is set to be higher than ADC full-scale so that the full ADC dynamic range can be utilized

5. DC offset and dynamic offset settling:





High gain VGA has the problem of amplifying DC along with incoming signal, resulting in headroom problems. A max static DC offset at the VGA output is usually specified, typically <1dB of ADC DR. Furthermore, when AGC is stepped up/down, a dynamic DC offset settling is specified as the time required for DC offset to settle below a max spec when the AGC is stepped.

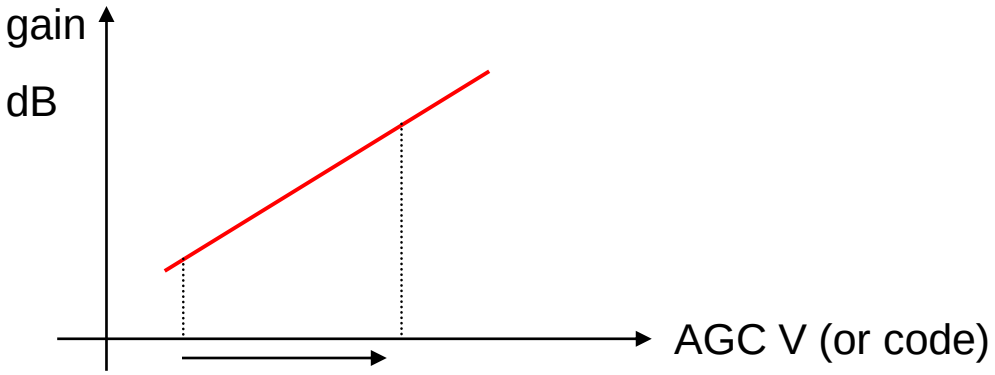
6. Misc.:

- out of band IP3, IP2. In some cases the VGA IP3/IP2 play a role in the overall receiver linearity and blocker spec. This happens if there is not enough out of band rejection at the baseband filter. A good example is CDMA system in a direct conversion architecture
- Inband IIP3 and IIP3 of VGA impacts signal SNR or EVM. In fact for WiFi 11ax MCS11 (1024QAM) it is one of the most challenging specs for a VGA/PGA
- VGA bandwidth not to cause a significant droop in the signal passband
- VGA highpass corner (for direct conversion, will be discussed later)

Note: because the VGA/PGA has variable gain, all these specs (noise, compression, DC offset, IIP3, etc need to be checked/guaranteed over the entire AGC range.

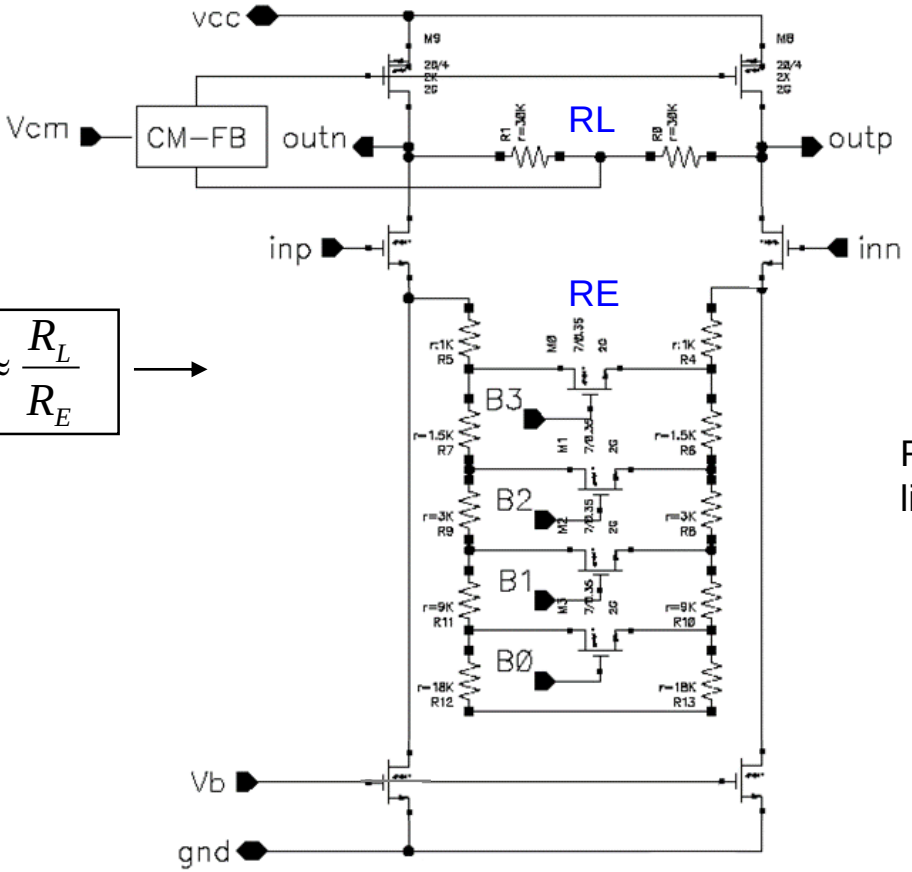
Linear dB/V or dB/code AGC control:

it is easier for DSP to deal with a linear dB/V or dB/code AGC to predict the change of AGC to realize a certain boost in received signal level.



For signal fading or signal search, the DSP changes the AGC to achieve a signal gain (usually in course increments first of 4~6dB followed by fine increments of 0.5~2dB) with a given search algorithm to get an optimum signal strength (set point of ADC). Linear dB/V with almost fixed slop with +/-1dB error over PVT is highly desired. This applies for both continuous or digital AGC.

Commonly used VGA topologies:

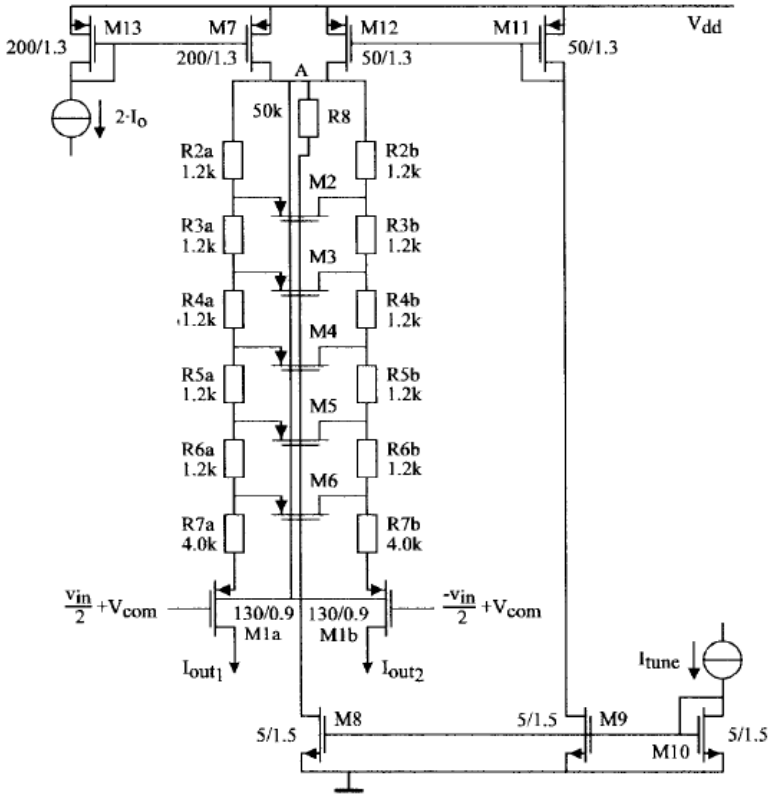


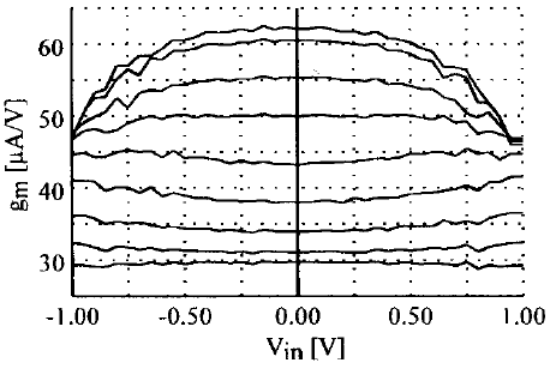
$$A_v \approx \frac{R_L}{R_E}$$

Resistors are scaled for linear dB/code response

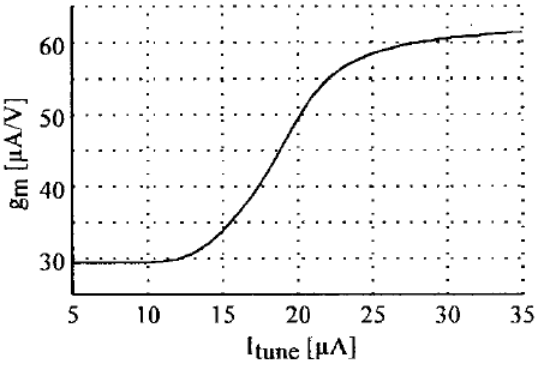
The variable degeneration resistor topology offers best compression vs. gain as well as noise. Linear dB/V is not easy to generate for continuous AGC.

Soft-switching continuous variable degeneration CMOS VGA:



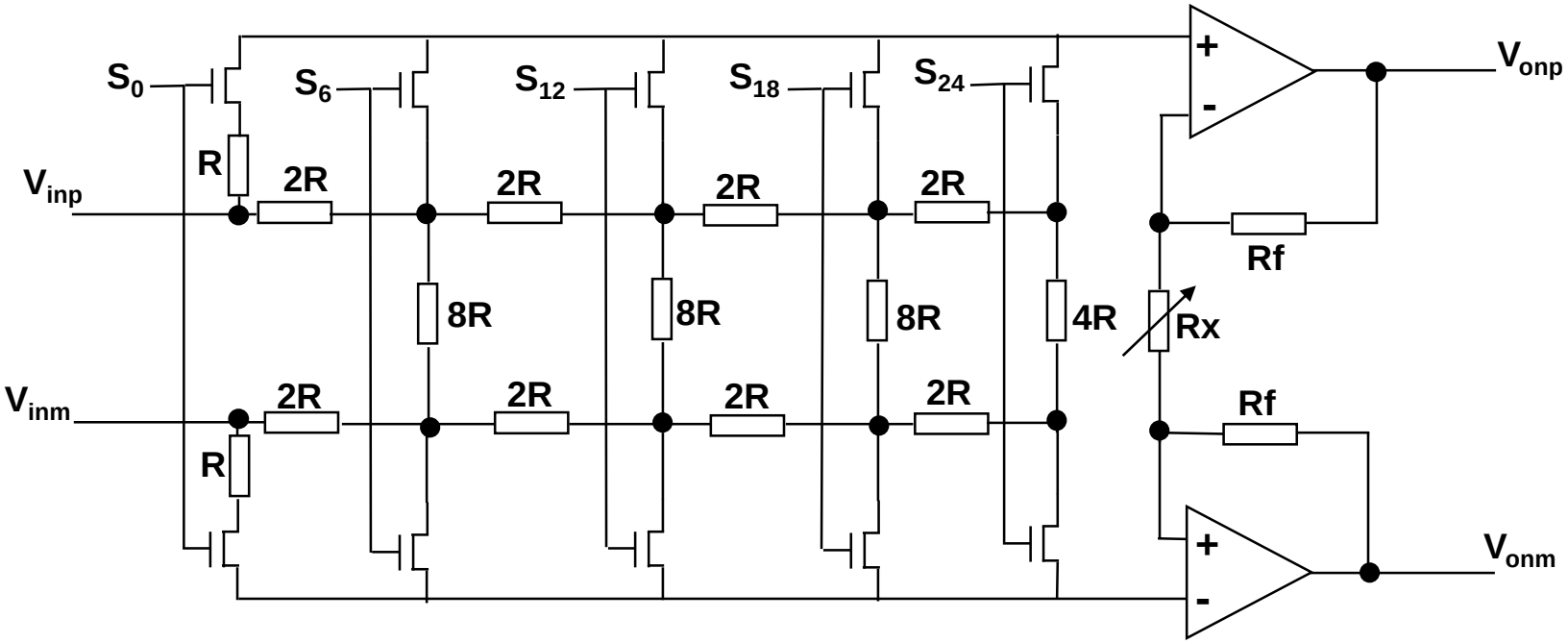


(a)



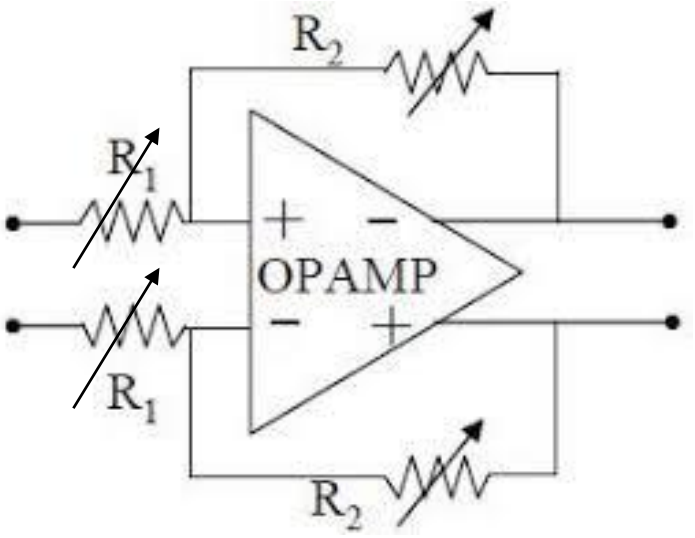
FETs are gradually turned on/off as the tune current/voltage increases/decreases. This provides a semi-linear control on gain. The tune/AGC voltage has to be distorted for linear/dB response [2]. Input compression increases as gain decreases (good)

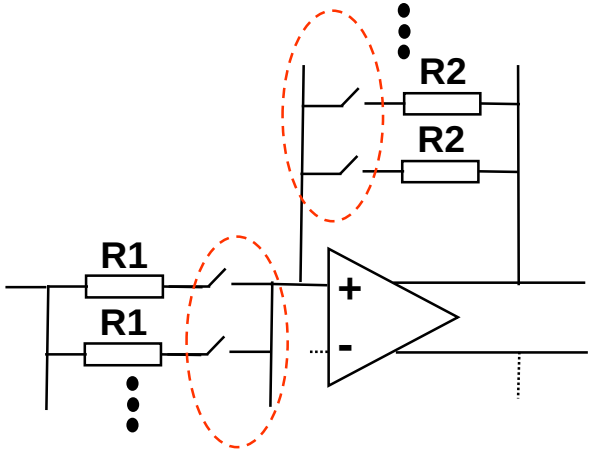
Programmable-gain CMOS amplifier (PGA):



S_0 to S_{24} AGC digital signals are active only one at a time. S_6 results in 6dB gain step, S_{24} results in 24dB gain step ..etc. Rx is made programmable with 1dB gain step and 5dB gain range to get an overall 30dB of AGC for this PGA. Input compression increases as gain decreases (good)

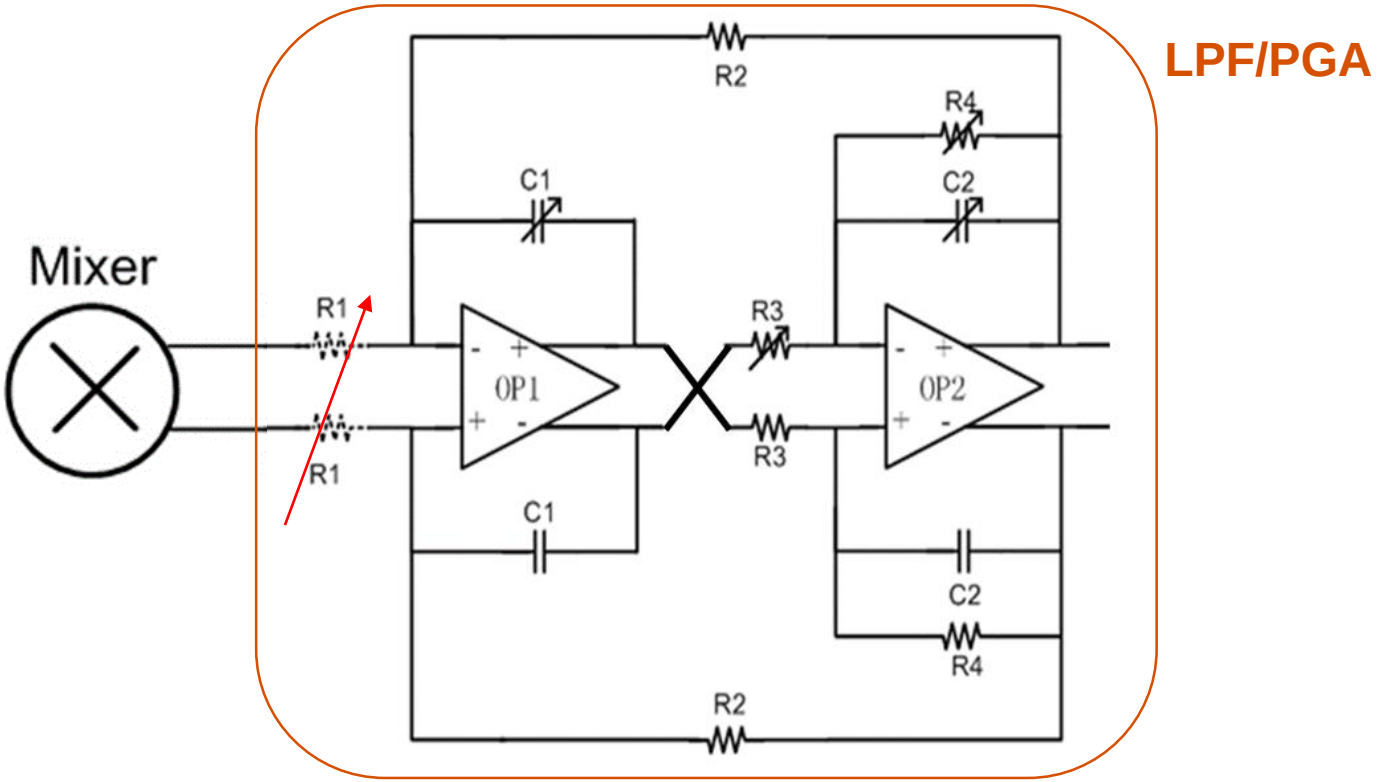
Programmable-gain CMOS amplifier (PGA):





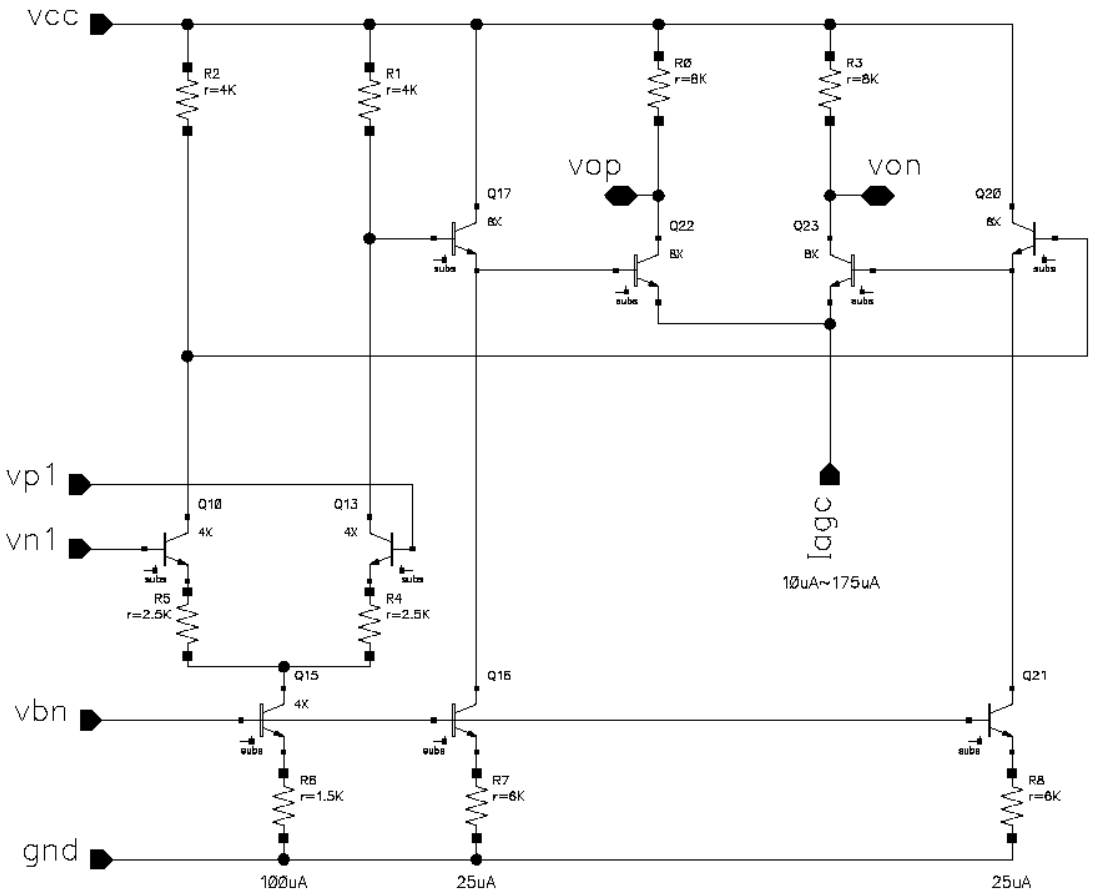
- R1 and or R2 are digitally programmable (resistor bank)
- Increasing R1 resuces Gain while input compression increases (good). Also noise increases as well
- reducing R2 requires better driving capability of the OPAMP. Usually fine gain step (say 1dB) with <3dB range is implemented in R2
- Please note that the switches used to program R1 or R2 are placed at the virtual ground side of the opamp to reduce the swing at their terminals and so their contribution to nonelinearity

Baseband filter as also PGA:



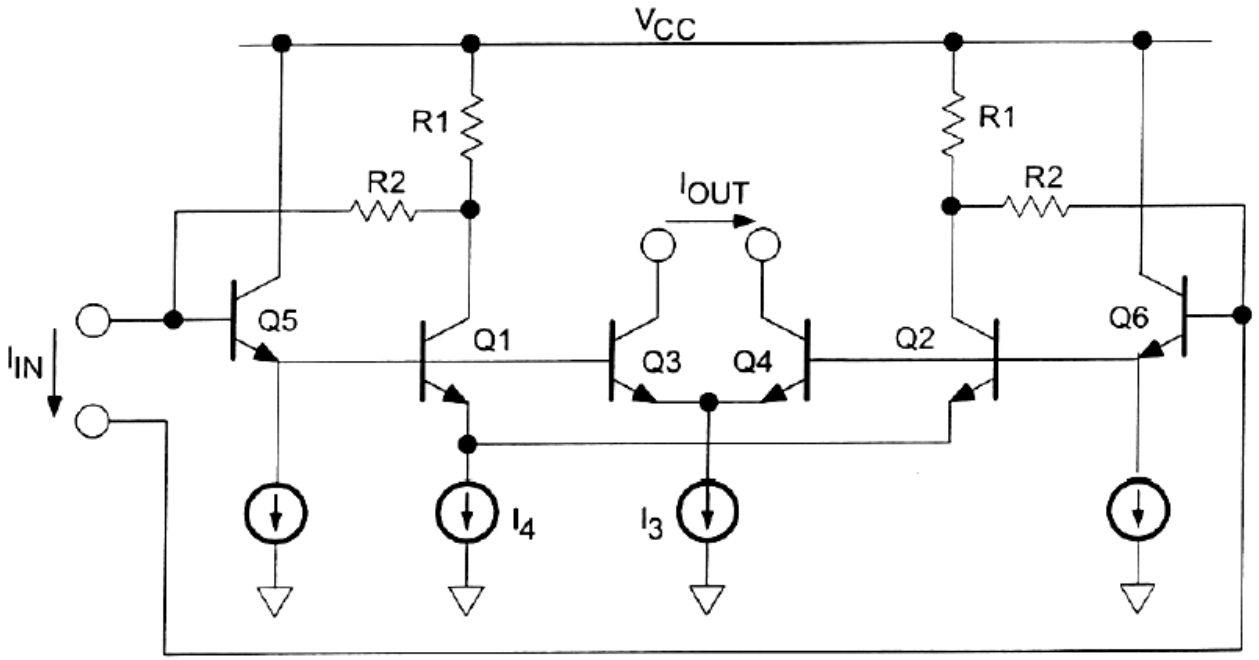
- Input resistor R1 of the filter converts input AC voltage (output of mixer TIA for example) into AC current due to OP1 virtual ground nodes. Therefore, changing the value of R1 (digitally via programmable resistors) changes the filter passband gain but it does not affect its AC response
- Such topology allows the LPF itself to also act as a PGA

Variable-gm VGA:



The variable Gm topology is simple and linear dB/V is easy to generate for continuous AGC. However compression vs. AGC is not good.

Improved variable-gm VGA:

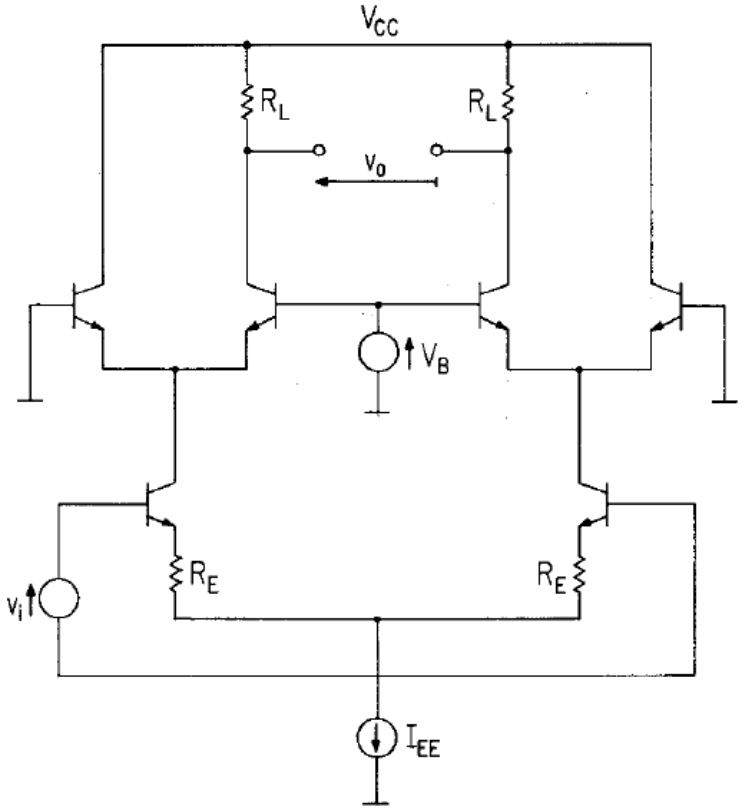


$$\frac{I_{OUT}}{I_{IN}} = \left(\frac{R2}{R1}+1\right)\left(\frac{I_3}{I_4}\right)\left(\frac{T}{1+T}\right)$$

$$T \sim gm_1 \times R1$$

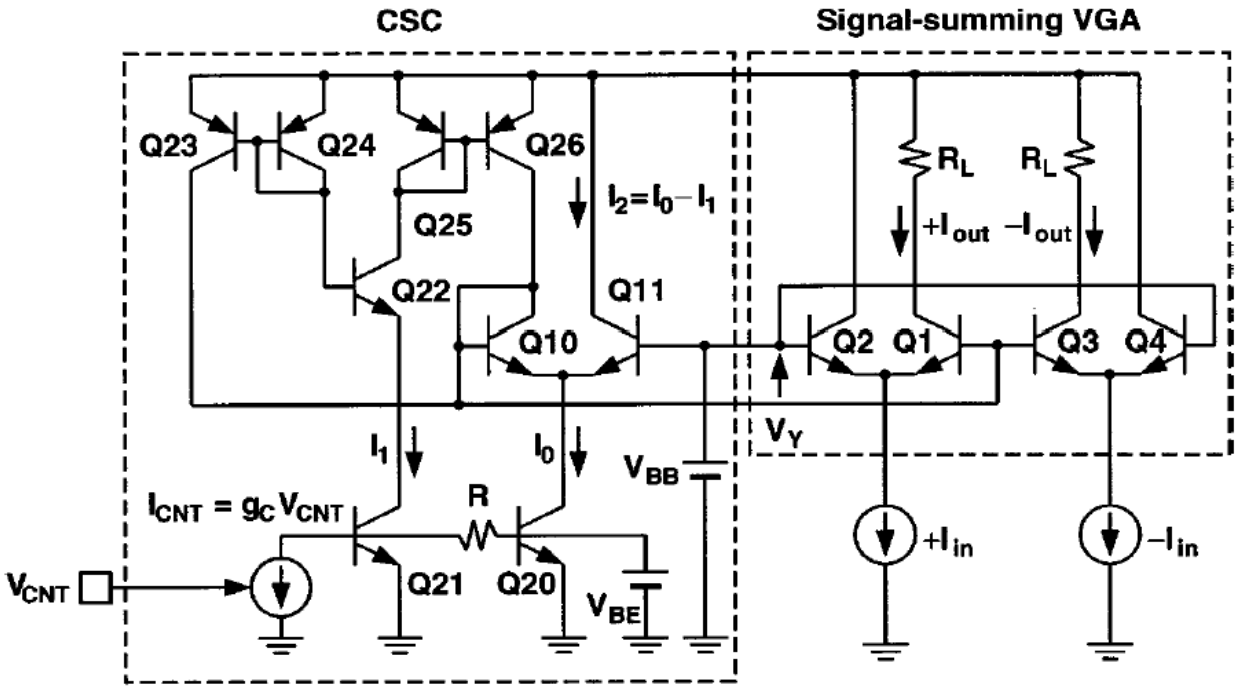
The modified variable Gm topology overcomes the shortcomings of the classic topology (compression vs. AGC). The variable inner and outer pair (I_3 and I_4) Gm is the key [3]

Current-steering VGA:



The Gilbert-cell type VGA has fixed input compression vs. AGC limited by the Gm stage. However, it is the most common VGA topology used.

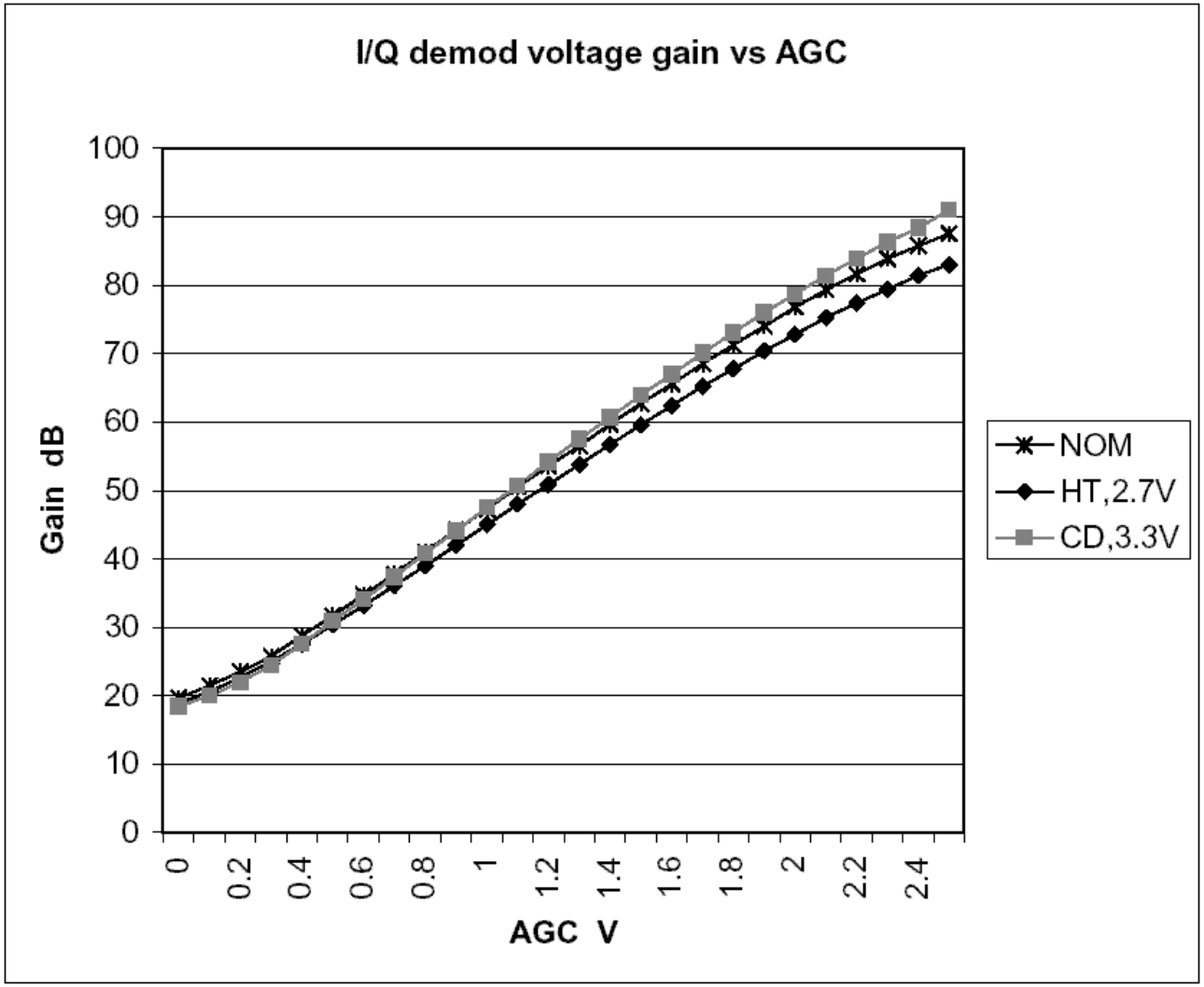
Linear dB/V AGC circuit for Current-steering VGA [4]:



$$V_Y = V_T \ln\left\{ e^{\frac{\alpha V_{CNT}}{V_T}} - 1 \right\} \quad ; \text{ where } \alpha \text{ is a constant}$$

$$\text{Gain} = Ke^{\frac{-RV_{CNT}}{V_T}} \Rightarrow Gain(dB) = 20\log(Gain) = K\frac{-R\alpha V_{CNT}}{V_T}$$

Measured gain vs. AGC for a variable Gm topology:



Appendix

Linear dB/V AGC for variable Gm topology:

$$V_{BE2} = V_{BE3} - RI_x \quad ; \text{ neglecting base current}$$

$$I_{AGC} = I_2 = MI_0 e^{\frac{V_{BE2}}{V_T}} = MI_s e^{\frac{V_{BE3}-RI_x}{V_T}} = MI_0 e^{\frac{V_{BE3}}{V_T}} e^{\frac{-RI_x}{V_T}}$$

$$\Rightarrow I_{AGC} = MI_{ref} e^{\frac{-RI_x}{V_T}}$$

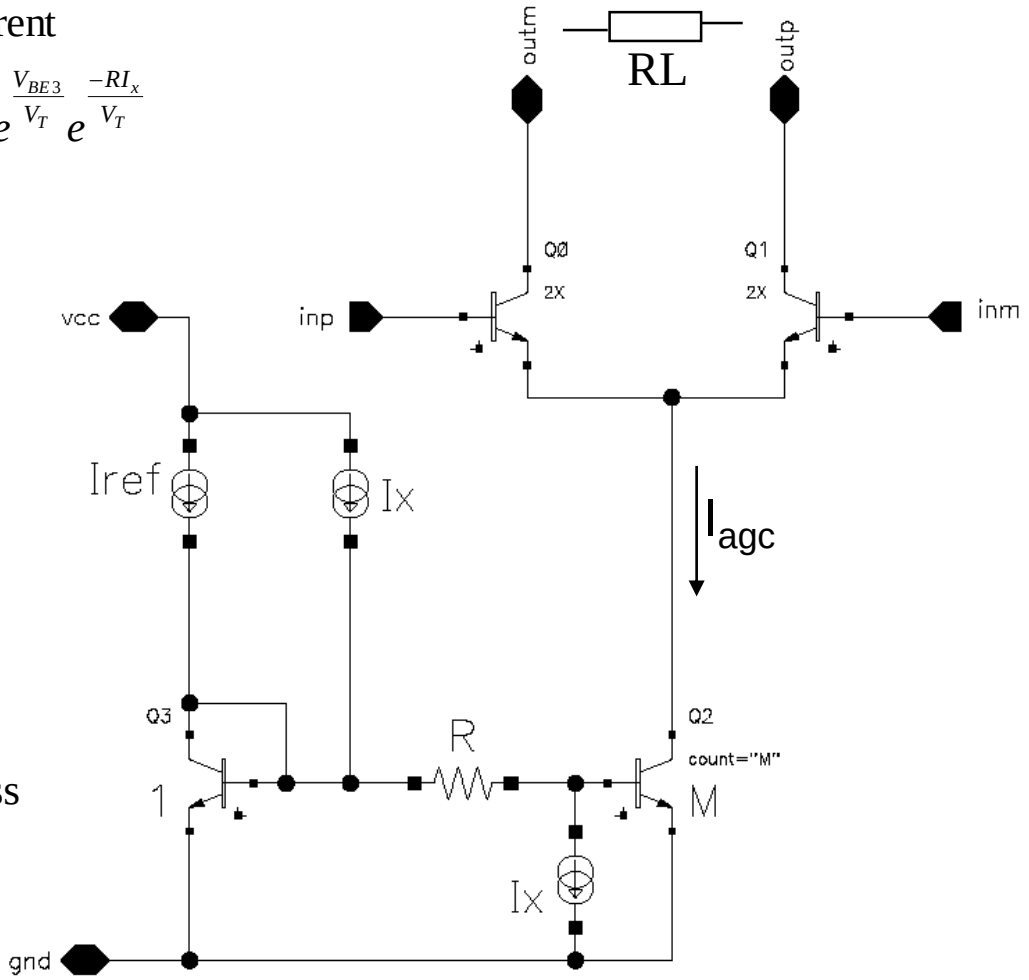
$$g_m = \frac{I_{AGC}}{V_T} = \frac{MI_{ref}}{V_T} e^{\frac{RI_x}{V_T}}$$

$$Gain = g_m R_L$$

- I_{ref} has to be PTAT referenced to same resistor as **RL** of the VGA for process independent gain

- I_x also has to be PTAT referenced to same resistor as ***R*** of the VGA for process independent gain control slope

$$\log(g_m) = k + \frac{R}{V_T \ln(10)} I_x$$



$$V_{od} = V_{op} - V_{om}$$

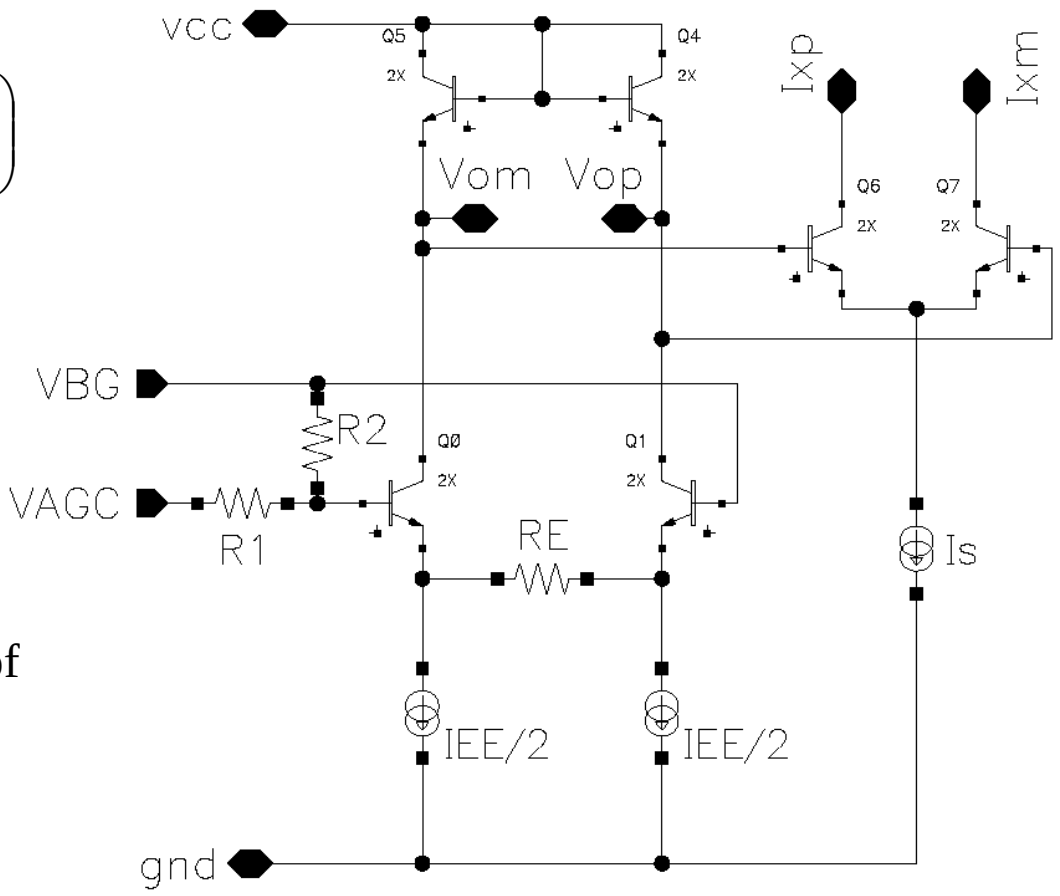
$$= 2V_T \tanh^{-1}\left(\frac{R_2}{R_1+R_2}\frac{V_{BG}-V_{AGC}}{R_E}\frac{1}{I_{EE}}\right)$$

$$I_{xd} = I_{xp} - I_{xm} = I_s \tanh\left(\frac{V_{od}}{2V_T}\right)$$

$$= I_s \frac{R_1}{R_1+R_2}\frac{V_{BG}-V_{AGC}}{R_E}\frac{1}{I_{EE}}$$

- I_S , (I_x), has to be PTAT referenced to same resistor as $\boldsymbol{R_L}$ of the VGA for process independent gain

- I_{EE} has to be BG referenced to same resistor as $\boldsymbol{R_E}$ for process independent AGC



References:

[1] W. Sansen, R. Meyer, “Distortion in Bipolar Transistor Variable-Gain Amplifiers,” IEEE JSSC, Vol. SC-8, No. 4, August 1973, pp. 275-282.

[2] C. Mensink, B. Nauta, “A CMOS Soft-Switched Transconductor and Its Application in Gain Control and Filters,” IEEE JSSC, Vol. 32, No. 7, July 1997, pp. 989-997.

[3] G. Sahota, C. Persco, “High Dynamic Range Variable-Gain Amplifier for CDMA Wireless Applications,” *in the Digest of ISSCC* 1997.

[4] S. Okata, G. Takemura, H. Tanomoto, “A Low-Power Low-Noise Accurate Linear-in-dB Variable-Gain Amplifier with 500MHz Bandwidth,” IEEE JSSC, Vol. 35, No. 12, December 2000, pp. 1942-1948.

[5] S. Reynolds, B. Floyd, T. Beukema, T. Zwick, “Design and Compliance Testing of a SiGe WCDMA Receiver IC with Integrated Analog Baseband,” Proceedings of IEEE, Vol. 93, No. 9, September 2005, pp. 1624-1636.