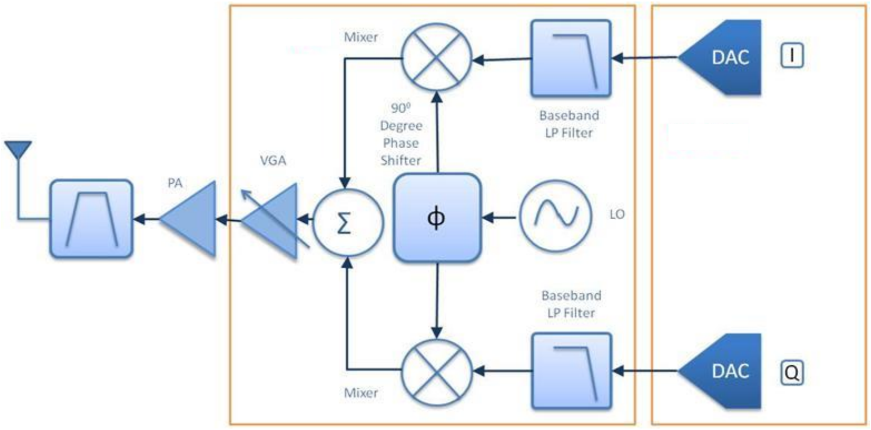
Transmitter Circuits

- **Transmitter circuits**
  - Important Tx specs (overview)
  - SAW-less transmitter challenge
  - Low-pass filter
  - Up-converter:
    - » Gilbert-cell
    - » Passive mixer
  - RF VGA/PGA circuits

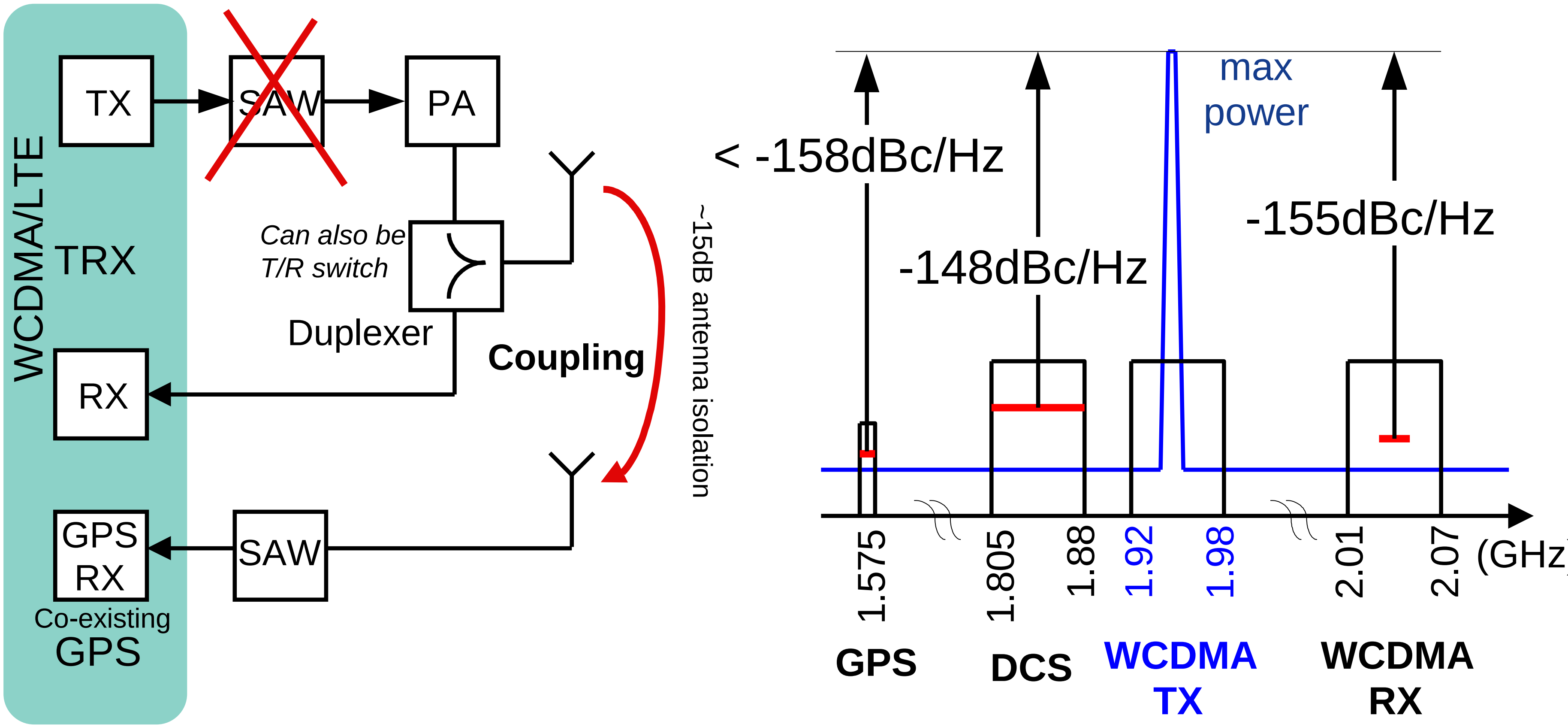
- **References**

Important specs for transmitter circuits (reminder)



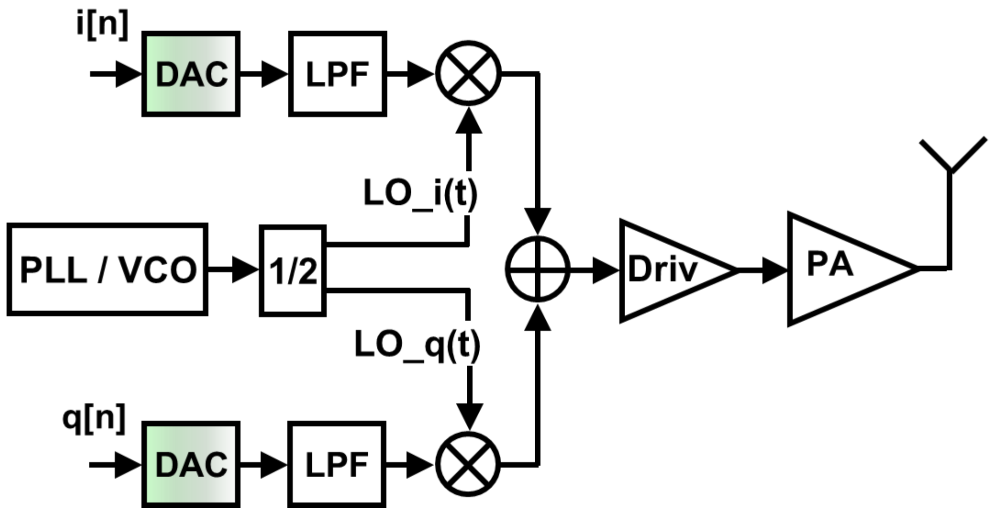
- **In-band linearity (IIP3, P1dB)**
  - Impacts signal SNR and EVM
  - Impacts emission mask
- **In-band noise**
  - Impacts signal SNR and EVM
- **Out-of-band noise**
  - Impacts out of band emission/mask
- **Baseband HD3/HD5/HDn**
  - Impacts out of band emission/mask
- **LO**
  - Integrated phase error (IPE) impacts signal SNR/EVM
  - Out of band phase noise and spurs impact emission
- **Misc.**
  - Pout, power control range (TPC), gain step
  - CIM3 and co-existence with other radios
  - Sideband suppression (IRR)
  - LO feedthrough

SAW-less transmitter challenge:



- Multiple radios need to operate simultaneously (for example cellular and GPS)
- Cellular Tx out of band noise (emission) can degrade GPS sensitivity → an off-chip SAW filter is added before cellular PA to remove emission in GPS band (>10dB below GPS sensitivity) while not degrading Tx output power

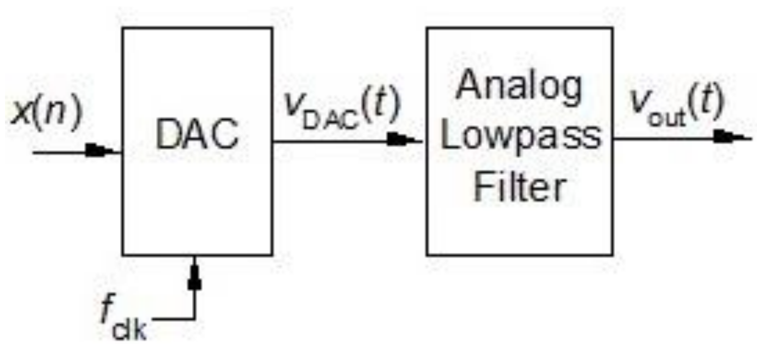
What is needed to remove the Tx SAW?

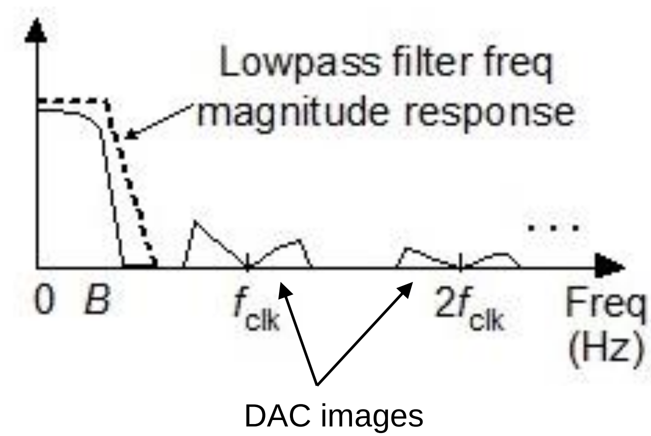


All impairments contributing to emission in the band of interest need to improve, with budgeting to each depending on difficulty in design:

- LO/PLL out of band phase noise
- Filter out-of-band noise and harmonic distortion (HD)
- DAC images (if they fall in that band, else DAC clocking is adjusted to avoid that band). Also DAC quantization noise (important for sigma-delta design)
- Tx chain out-of-band noise
- Tx chain out-of-band distortion (especially CIM3)

Objective of a Low-pass filter in a transmitter:

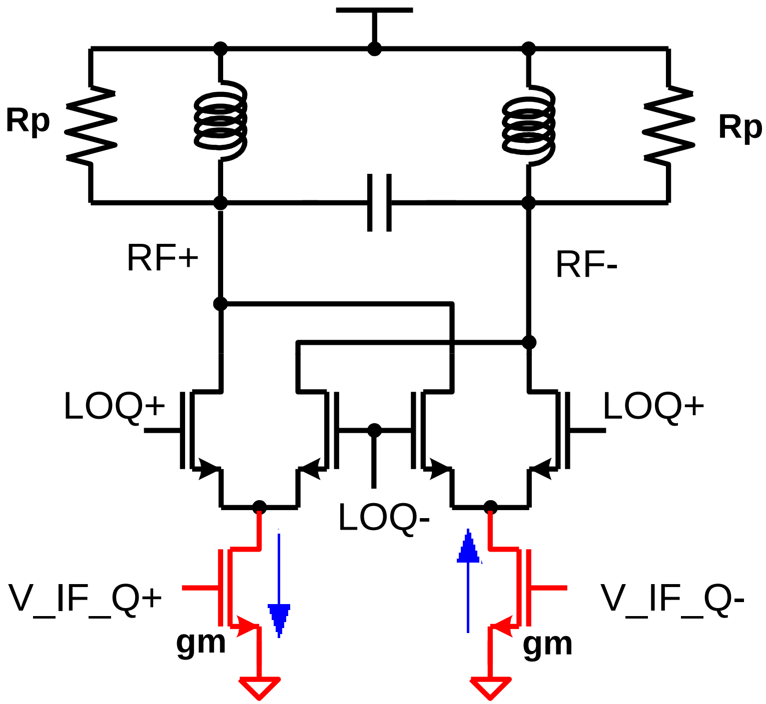




The lowpass filter in a transmitter (DCT) is mainly to:

- convert DAC current into voltage and/or to properly interface to the DC-coupled up-converter circuit (in some cases)
- filter out DAC images (for Tx out of band emission requirement)
- provide fine gain control (<3dB range with <=1dB steps)
- the lowpass filter out of band noise is extremely important because it also affects Tx out of band emission.
- As discussed before, its in-band distortion, group delay ripple, passband droop, etc affect signal integrity (EVM)

Up-converter circuits: Gilbert-cell



$$\overline{v_{n\_out}^2} = \left(\frac{2}{\pi}\right)^2 4KT\gamma g_m R_p^2 + 4KTR_p$$

$$= 4KT\gamma \frac{G_v^2}{g_m} + 2\pi KT \frac{G_v}{g_m}$$

Where $G_v = \frac{2}{\pi} g_m R_p$

↓*noise* ➔ ↑gm ➔ ↑Power

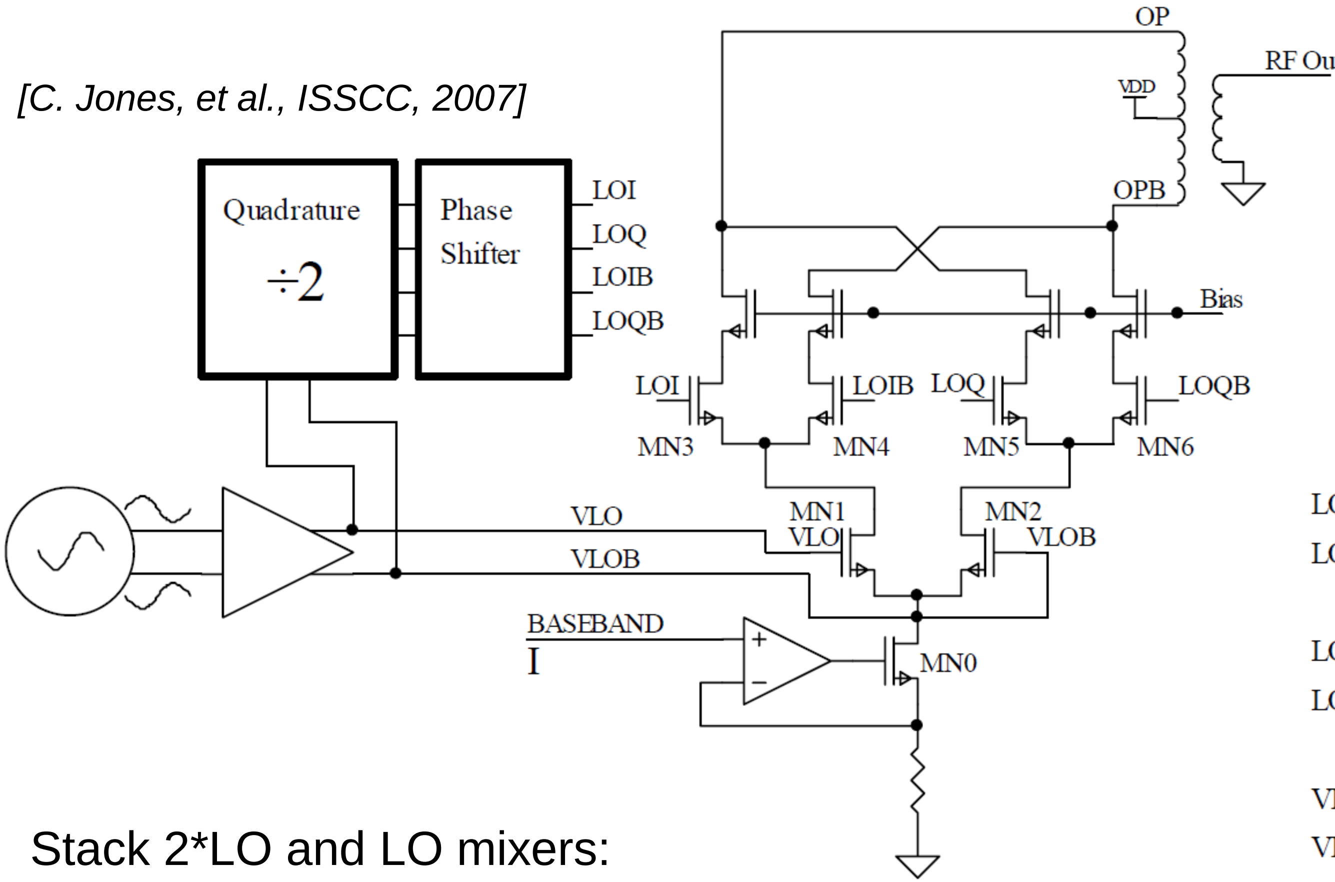
Limitation of Gilbert-cell up-converter:

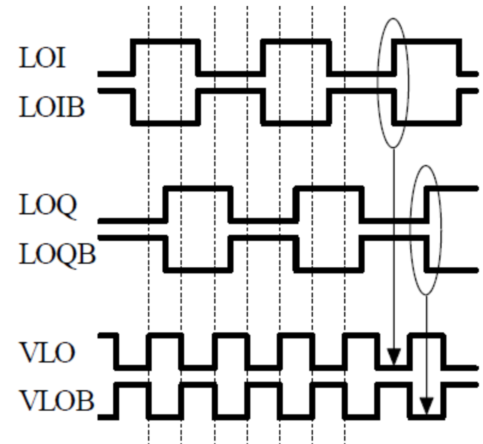
- V-I converter is noisy (large power consumption is needed to lower noise)
- Linearity is limited by the V-I conversion of gm stage
- LO transition significantly degrade noise from switching devices

→ Maybe unsuitable for SAW-less design

Up-converter circuits: improved Gilbert-cell

[C. Jones, et al., ISSCC, 2007]



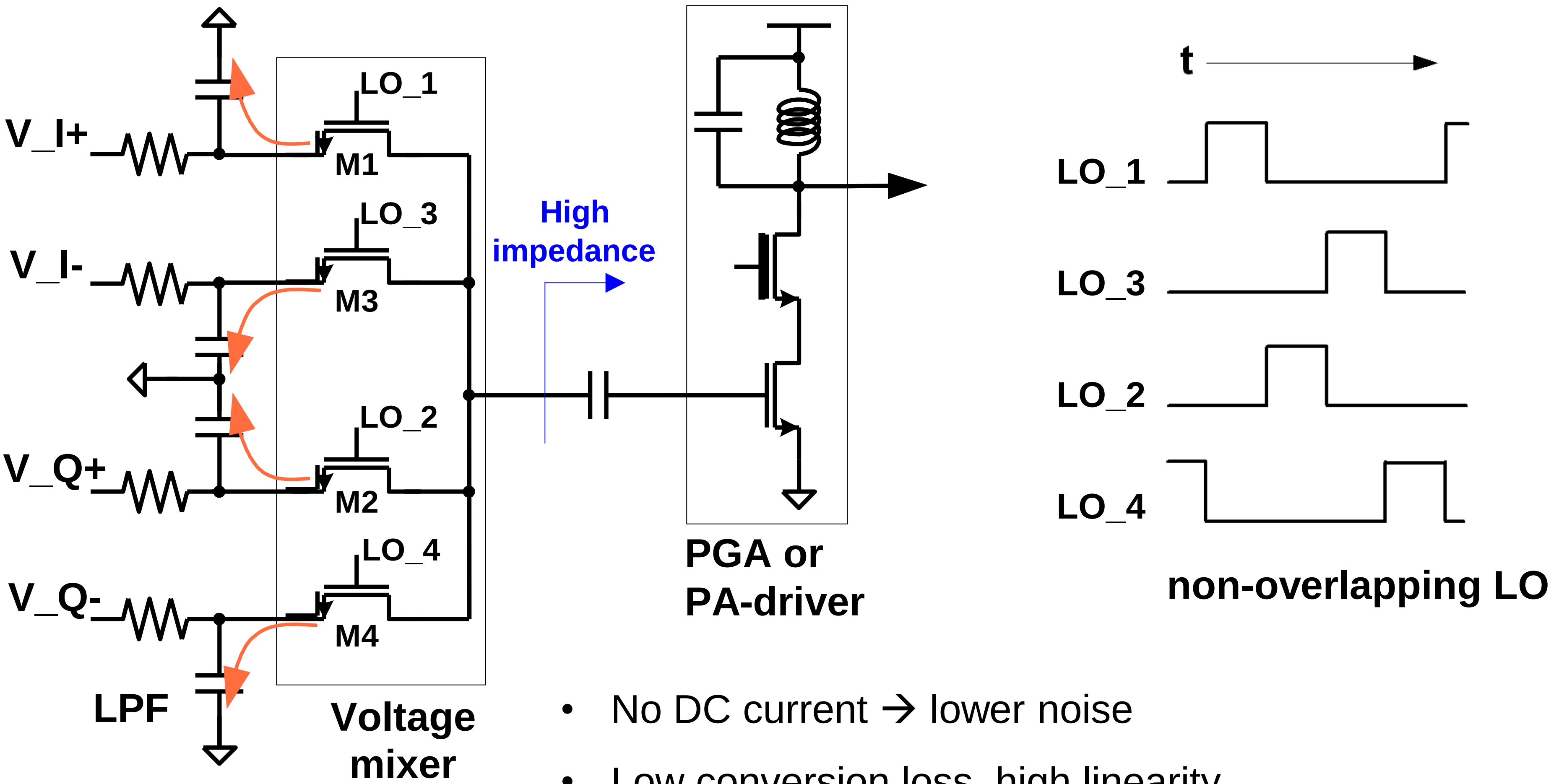


Stack 2*LO and LO mixers:

- It is effectively a 25% LO scheme which reduces noise from switching devices
- Linearity and noise is still limited by the V-I conversion of gm stage
- Headroom issue

→ Worked for SAW-less design but at large current

Up-converter circuits: voltage passive mixer with 25% LO

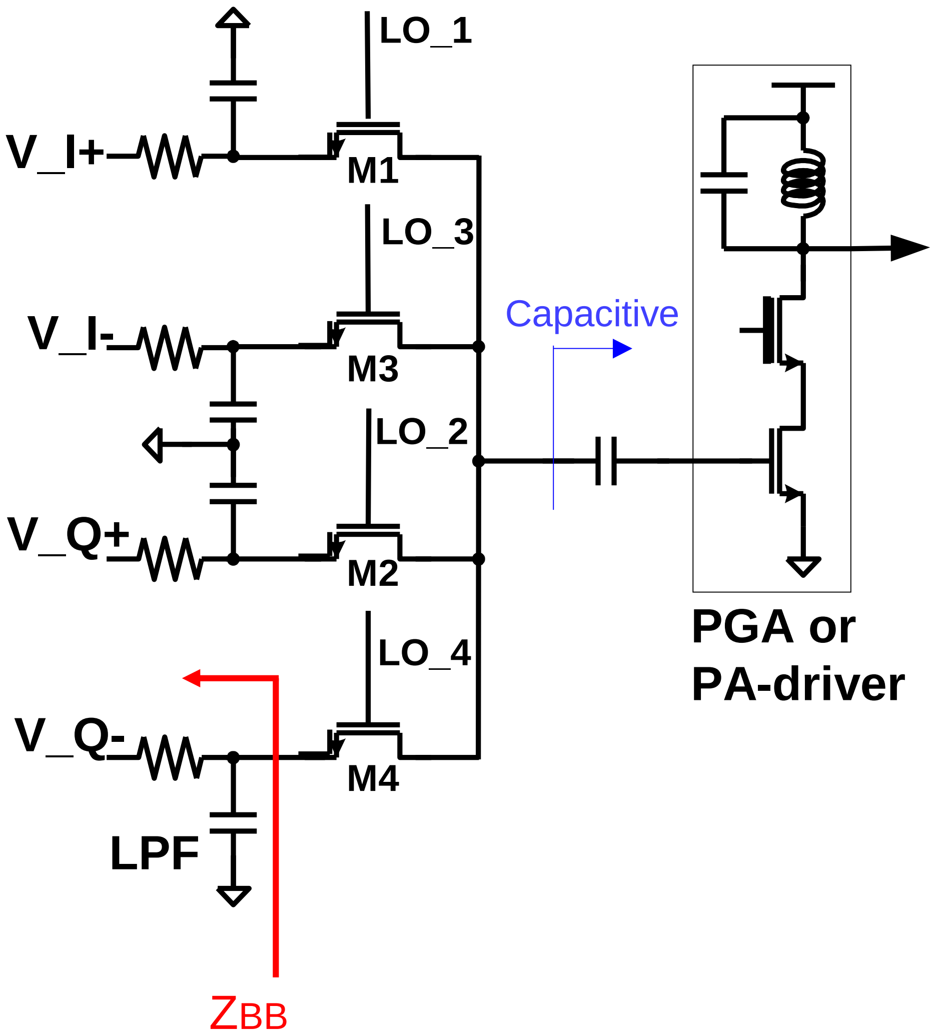


[X. He, et al., ISSCC, 2009]

- No DC current → lower noise
- Low conversion loss, high linearity
- LO spikes absorbed by BB RC filter

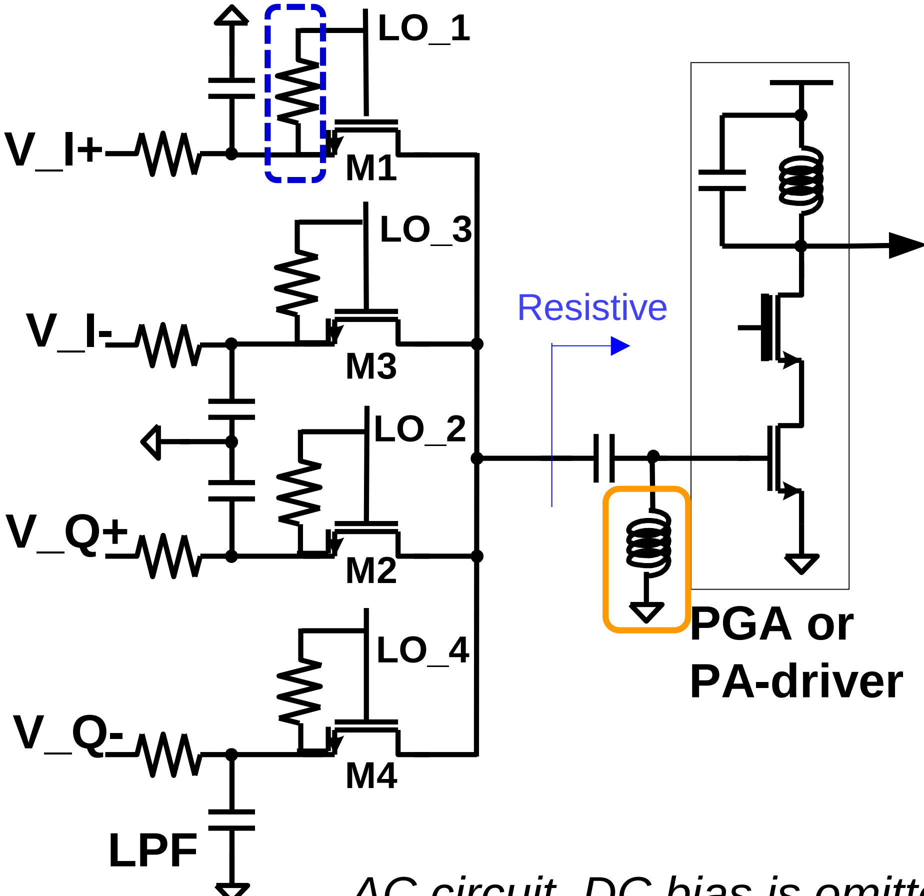
→ Works well for SAW-less design

Voltage passive mixer with 25% LO: important issues



- mixer linearity degrades vs large baseband swing due to varying Vgs
- The PGA/PAD circuit input impedance is mainly capacitive. The baseband circuit needs to charge this cap over a very short 25% LO period to avoid distortion. This puts a stringent ultra-low impedance requirement on baseband driving impedance Z_{BB}
- The capacitive nature of PGA/PA impedance causes upper/lower side bands of the transmitted spectrum to have a tilt (uneven) → degraded sideband suppression + passband droop.

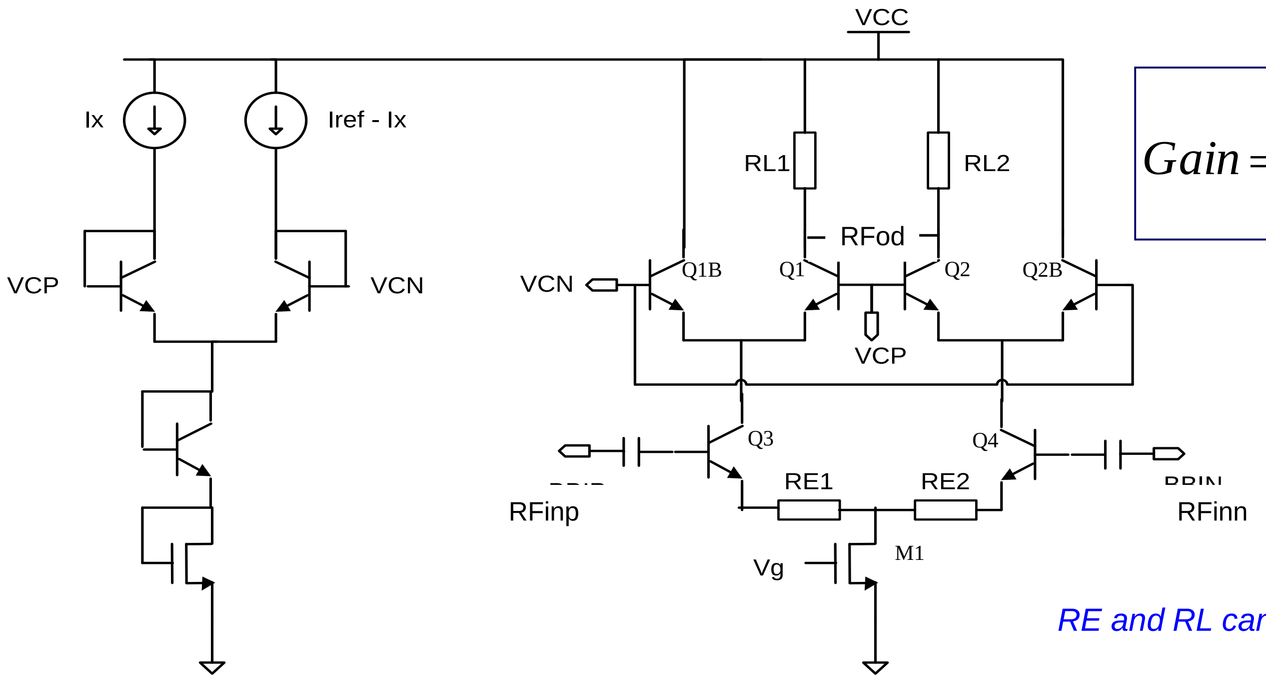
Voltage passive mixer with 25% LO: solutions



AC circuit. DC bias is omitted

- A bootstrap resistor is added between baseband and LO terminals to help improve mixer linearity vs large baseband swing
- A balun or resonance inductor at PGA/PA input is needed to resonate out the capacitive component of its input impedance. This shall relax the baseband circuit driving capability requirement as well as improves the upper/lower sideband tilt issue

RF VGA: current steering



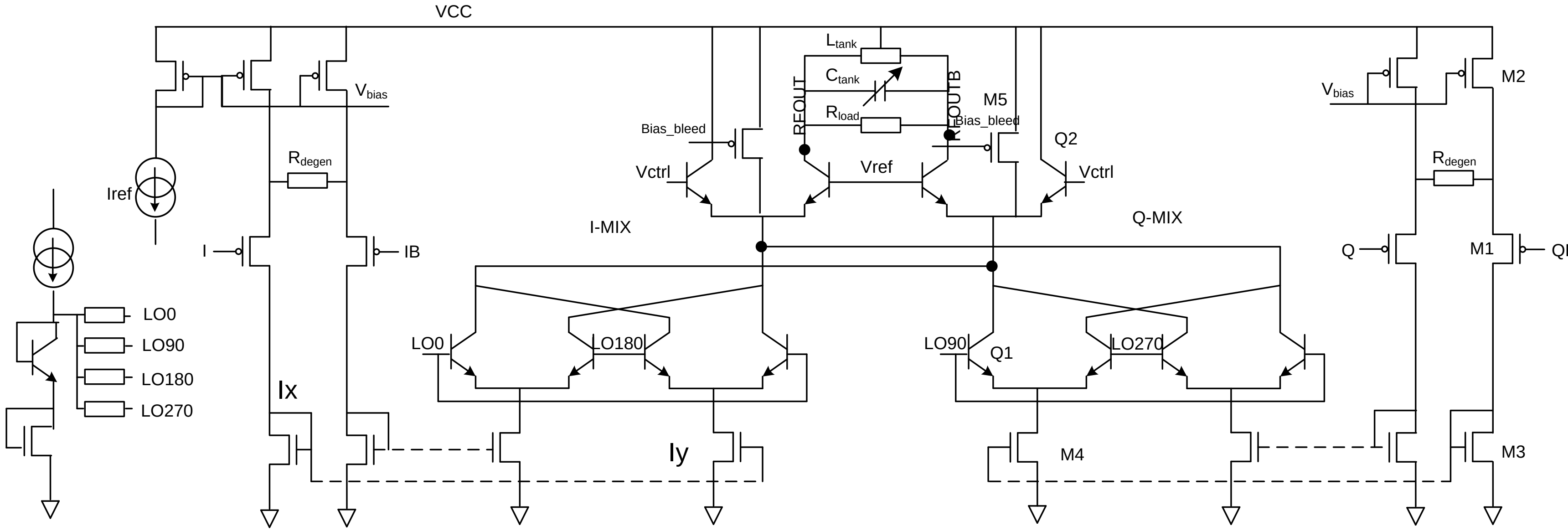
$$Gain = \frac{g_{mQ3,4} R_{L1,2}}{1 + g_{mQ3,4} R_E} \times e^{-\left(\frac{I_{ptat} V_{ctrl}}{I_{const}} \cdot \frac{1}{V_T}\right)}$$

Linear-in-dB characteristic

RE and RL can be replaced by inductors

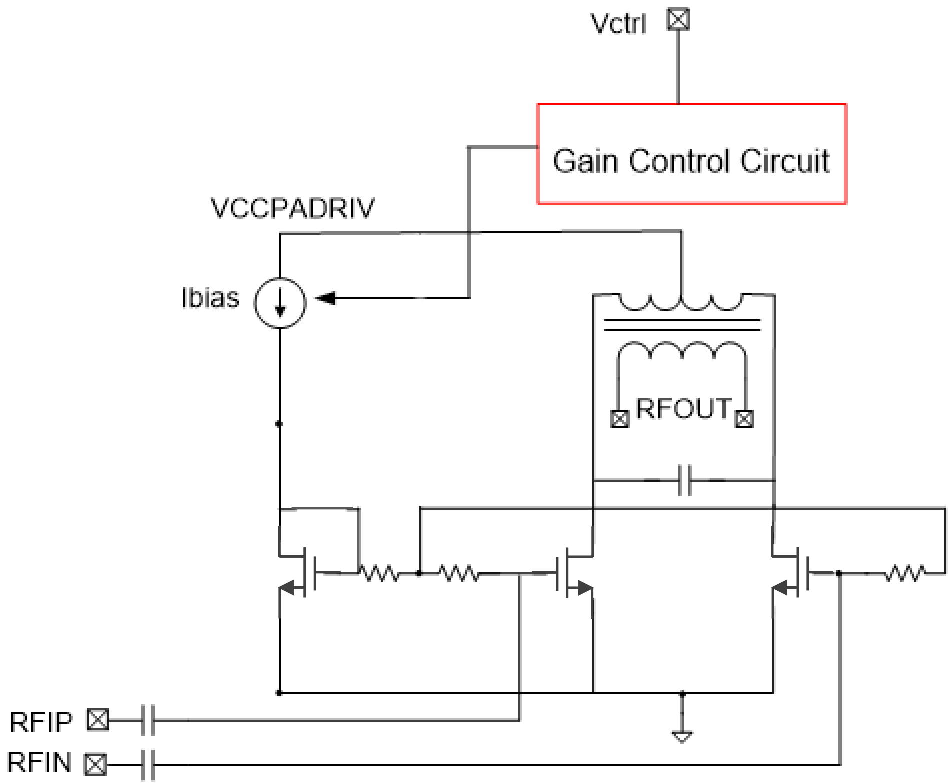
- Gain control is done by changing Ix (Vctr generates Ix in another linear Gm cell). MOS circuit is exactly the same, except the control voltage Vctrl that generates Ix is designed based on the process node to get linear-in-dB gain behavior
- Current consumption is fixed over gain control (not desired in Tx design)
- Lowest achievable gain is limited by isolation between input and output of VGA

Stacked mixer and VGA: current steering



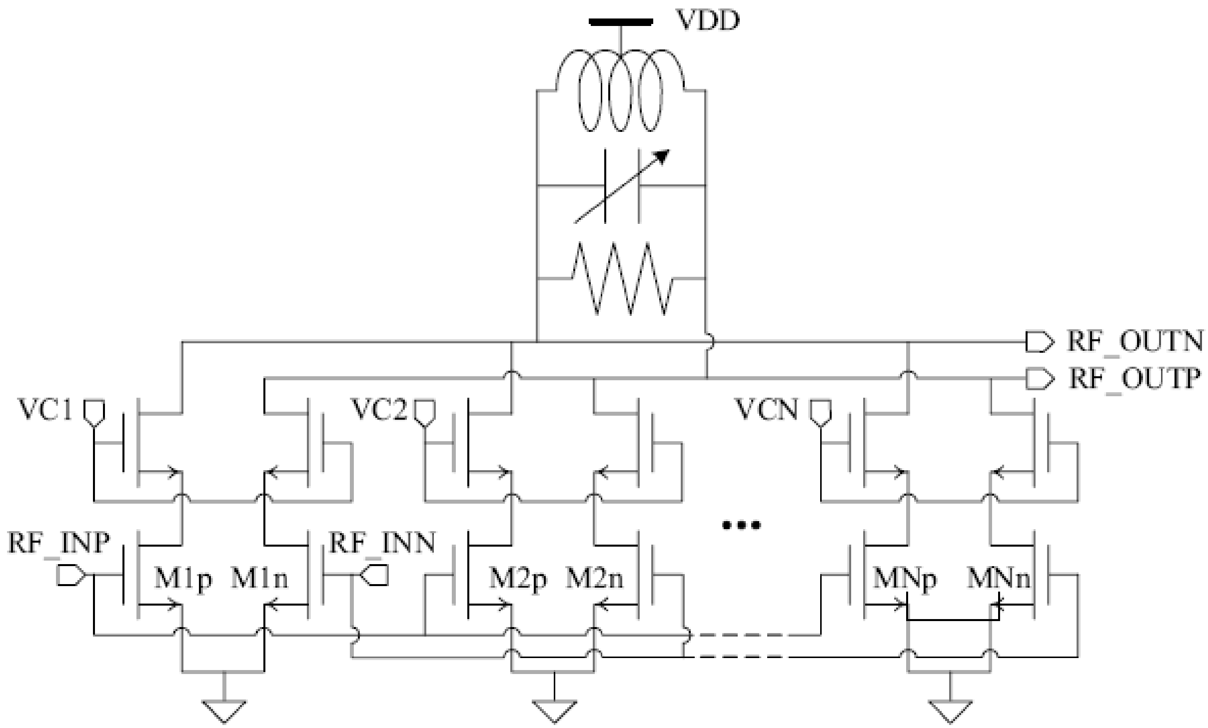
- Current-reuse → saves power consumption
- Headroom issue
- Potential stability issue due to throw-away current leaking back to VGA input
- An all-CMOS circuit is very similar except the current-steering section is usually sliced with device ratio done in away to get a linear dB/code gain (digitally controlled)

VGA: bias current change



- VGA/PGA current is adjusted to give linear/dB gain behavior (can be digitally controlled)
- Total VGA/PGA Current reduces vs gain control (good)
- VGA input compression reduces as gain drops (need careful level plan)

PGA: slicing



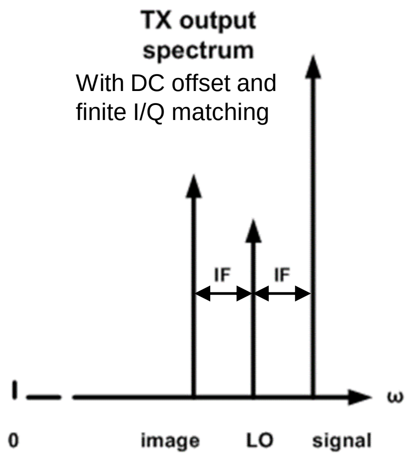
- Gain control is achieved by digitally switching on/off cascode transistor bias
- Transistors' ratio (slicing) is set to get linear-in-dB vs gain control code
- Current consumption drops vs gain control (good)
- Device current density remains constant vs gain control and so does PGA input compression

Transmitter Calibrations:

Things to calibrate:

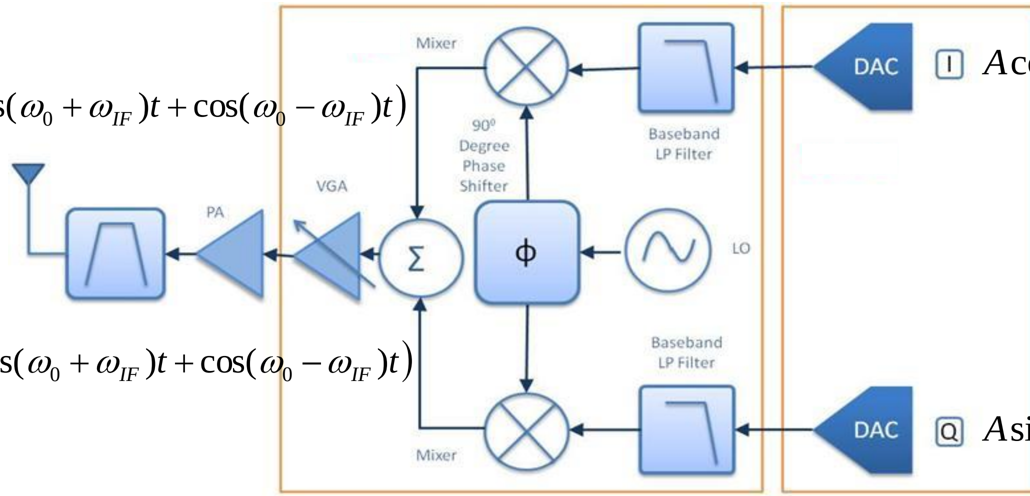
- LO feedthrough (LOFT)
- Frequency Independent/Dependent (FI/FD) Sideband (image) suppression
- Absolute gain and gain steps
- TSSI

LO feedthrough and FI Sideband suppression calibration



$$\frac{A}{2}\left(\cos(\omega_0+\omega_{IF})t+\cos(\omega_0-\omega_{IF})t\right)$$

$$\frac{A}{2}\left(-\cos(\omega_0+\omega_{IF})t+\cos(\omega_0-\omega_{IF})t\right)$$



$A\cos(\omega_{IF}t)$

$A\sin(\omega_{IF}t)$

if there is DC offset in baseband circuits, you get at RF:

$$RF_{out}=DC_{offset}\times LO=DC_{offset}\cos(\omega_{LO}t)$$

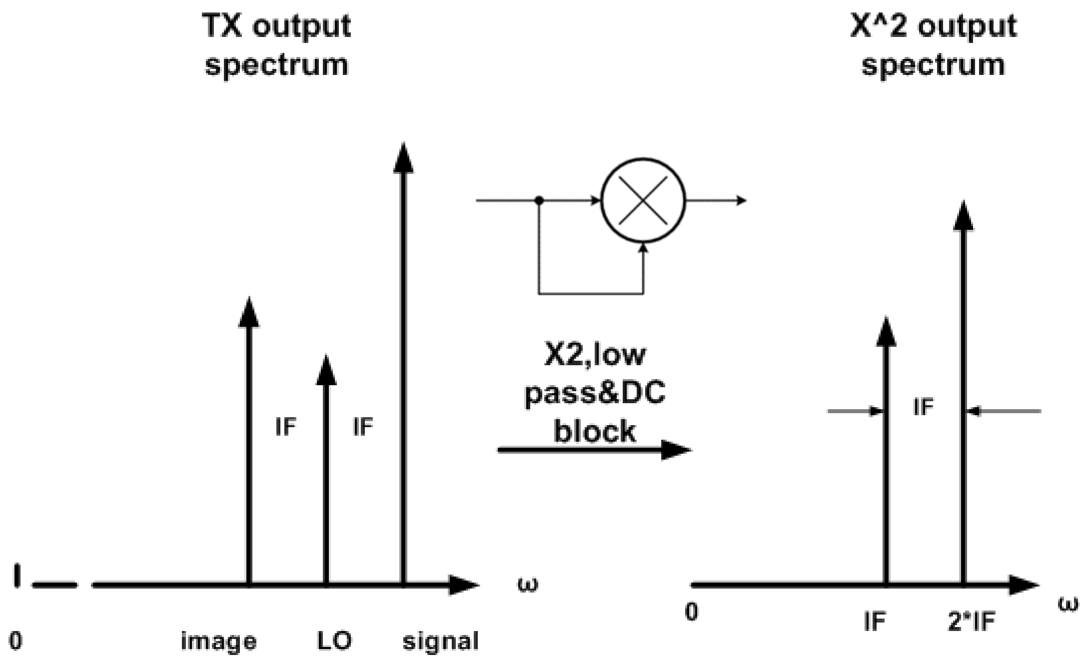
if there is gain (and/or phase) imbalance between I and Q signals, you get:

$$RF_{out}=A\cos(\omega_{LO}+\omega_{IF})t+\delta A\cos(\omega_{LO}-\omega_{IF})$$

With δ is the I/Q gain imbalance (you can repeat the math for phase imbalance)

- For calibration, we inject a baseband CW tone at some IF offset from LO and the spectrum can then be used for calibration as follows

LO feedthrough and FI Sideband suppression calibration



$$S_d = A_d cos(\omega_0 + \omega_{IF})t$$
$$S_{LO} = A_{LO} cos(\omega_0)t$$
$$S_{IM} = A_{IM} cos(\omega_0 - \omega_{IF})t$$

$$v_{in} = S_d + S_{LO} + S_{IM}$$
$$v_{in}^2 = (S_d + S_{LO} + S_{IM})^2$$

After lowpass filter:

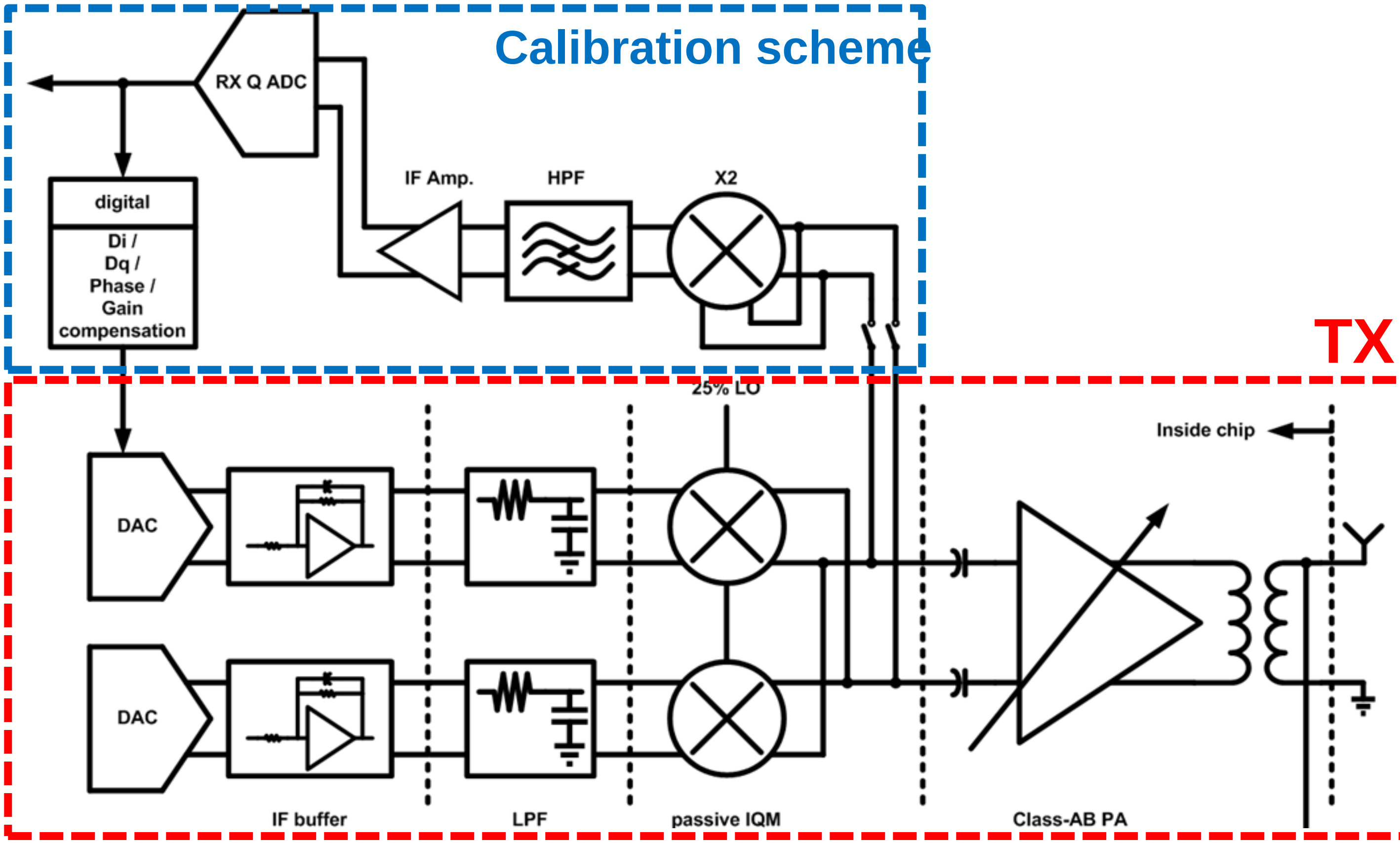
$$v_{in}^2 = DC + \frac{1}{2}[A_d A_{LO} + A_{IM} A_{LO}]\cos(\omega_{IF})\,t + \frac{1}{2}[A_d A_{IM}]\cos(2\omega_{IF})\,t$$

$A_{IM}A_{LO} << A_d A_{LO}$

$$\rightarrow v_{in}^2 \approx \overbrace{\frac{1}{2}[A_d A_{LO}]\cos(\omega_{IF})\,t}^{LOFT} + \overbrace{\frac{1}{2}[A_d A_{IM}]\cos(2\omega_{IF})\,t}^{image}$$

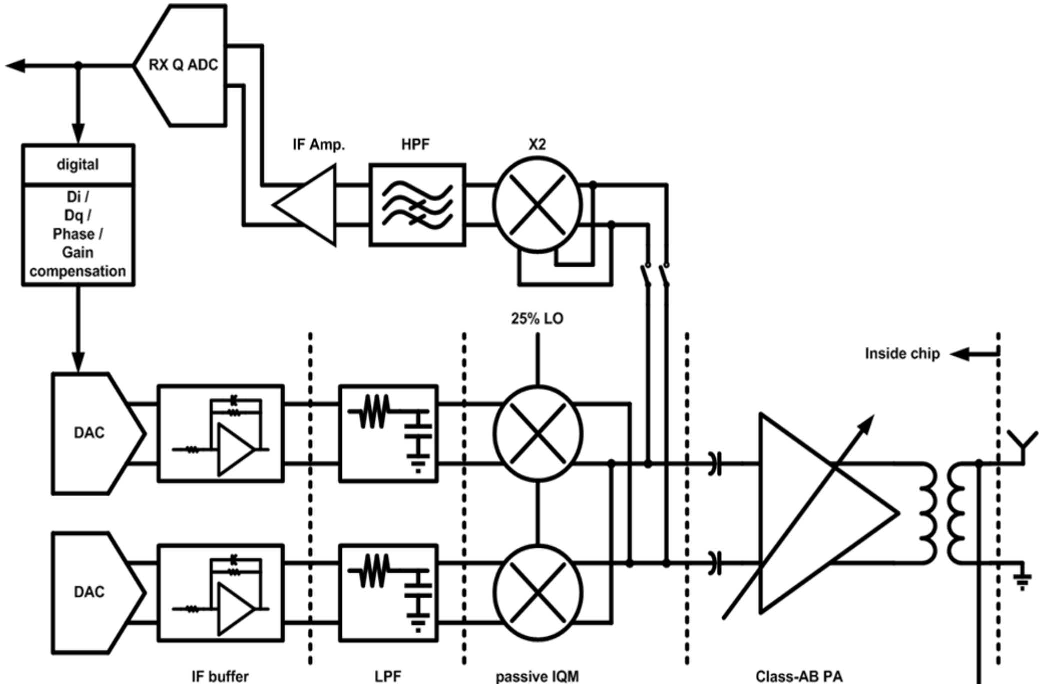
- Squaring the transmitted CW signal generate components at baseband that are proportional to LOFT and SB signals which are fed to an on-chip ADC (usually the Rx's)

LOFT and image calibration scheme



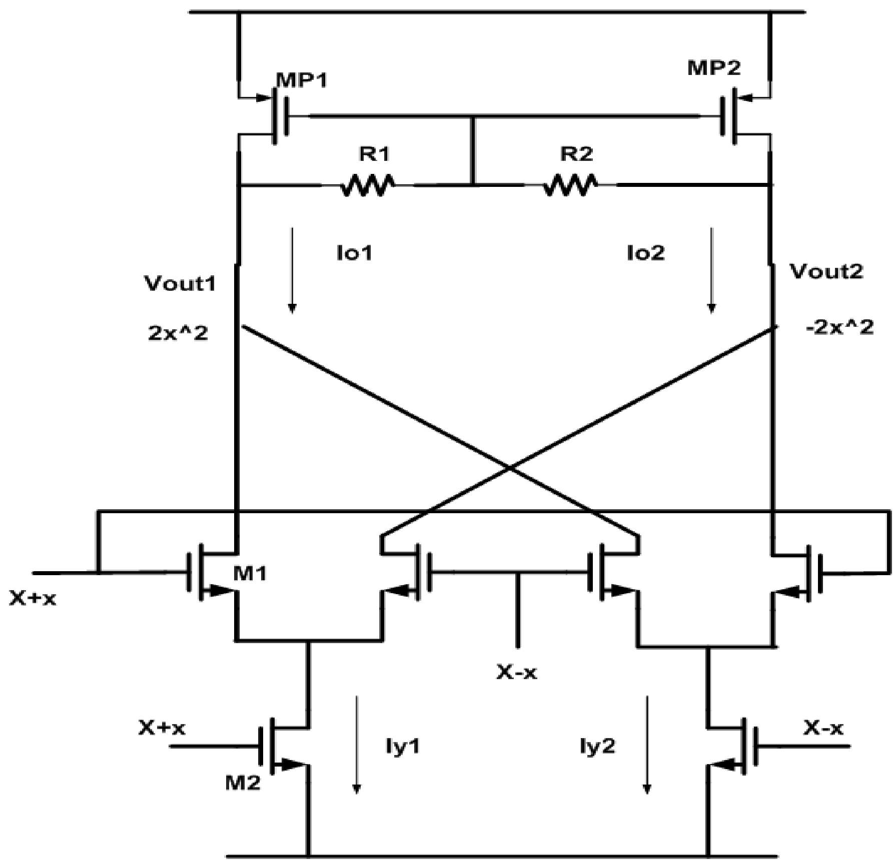
- Squaring circuit input can be taken from up-converter output or PA-driver output. An attenuator circuit maybe needed to lower swing at its input
- Squaring circuit output is AC coupled to a lowpass filter then to the receiver ADC. A digital algorithm adjusts the DAC offset current to lower LOFT. It also adjusts the I/Q mag/phase to suppress the component at 2IF.

LOFT and image calibration scheme specifications



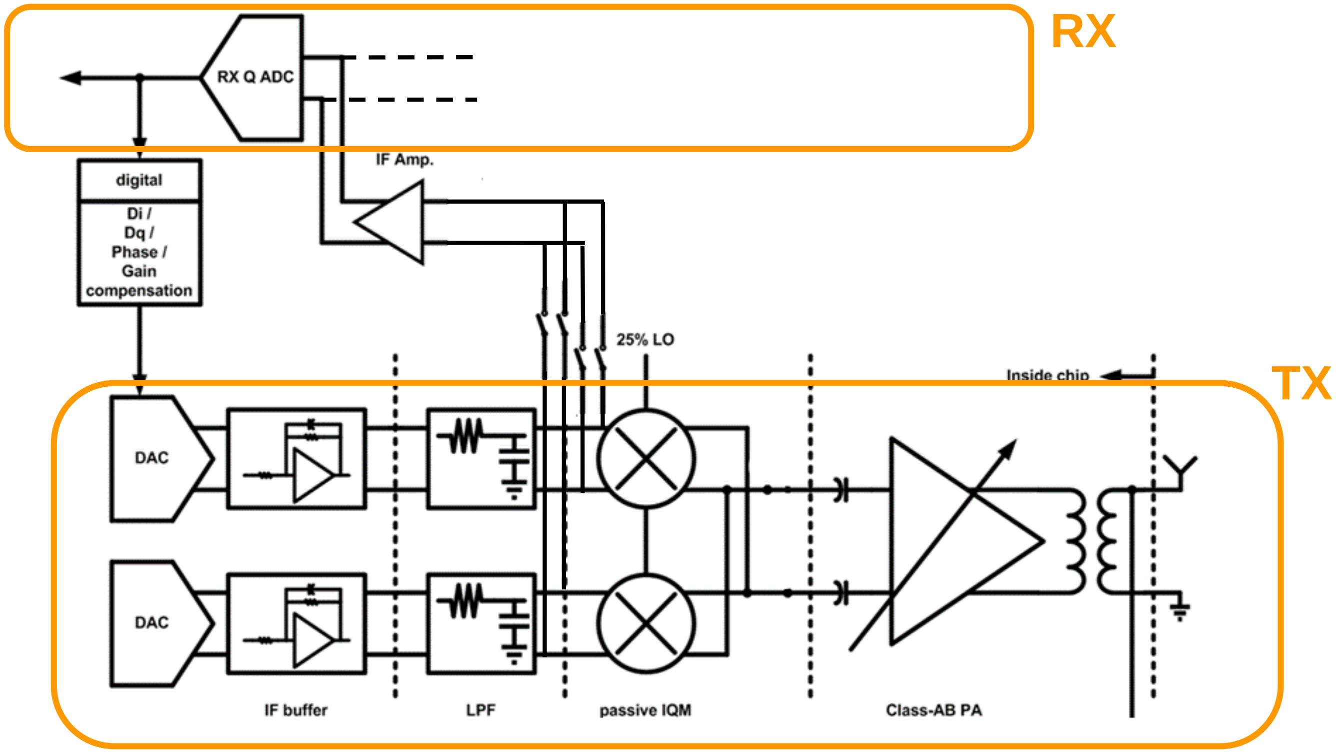
- Scheme must calibrate LOFT and SSB for all Tx gain settings. Usually LOFT is sensitive to analog baseband circuit gain (LPF for example) than RF gain.
- The SNR at the ADC out of the calibration scheme must be met so that digital circuit does not need to do extensive averaging (increases calibration time).
- Calibration table (gain setting, LOFT cal setting, SSB cal setting) is stored into none-volatile memory inside the SoC and is loaded by firmware upon power up

Squaring circuit:



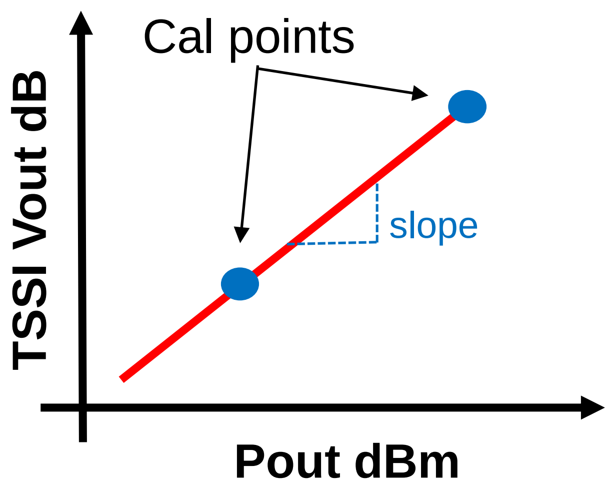
- Gilbert-cell mixer is a good candidate for the squaring circuit with Tx signal connected to both inputs.
- Load network is designed so that gain of this circuit remains relatively flat over PVT for easier calibration procedure

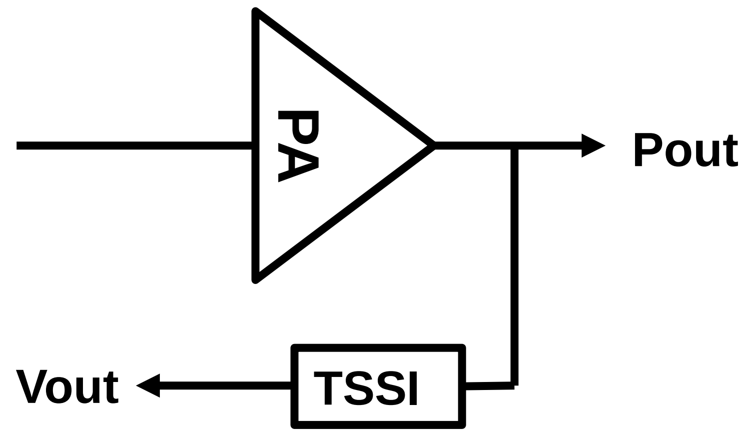
FD image calibration scheme:



- Frequency Dependent (FD) sideband (image) is caused by Tx baseband filters.
- Tx digital BB injects a CW I/Q BB tone in-band. The Tx LPF out is sent to Rx ADC and I/Q are compared. The CW tone frequency is swept over the Tx baseband bandwidth and for each BB frequency the I/Q matching is recorded.
- Tx digital engine compensates I/Q gain and phase in an inverse way to calibrate this FD IRR
- Please note that the same ADC is used to measure Tx I and Q signals to eliminate and error due to ADC itself.

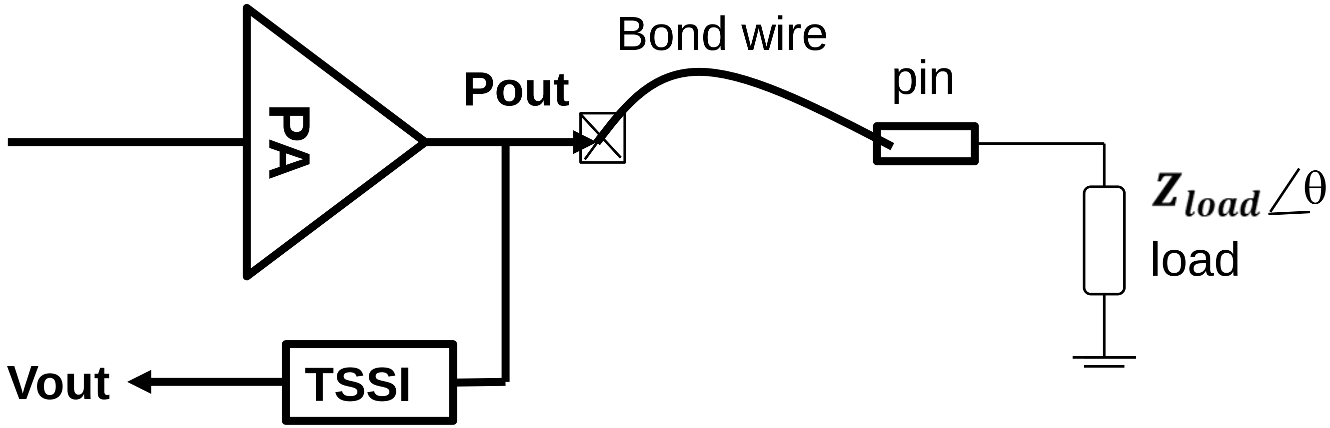
Tx gain/Pout calibration and TSSI:





- In some systems, absolute transmitted power need to be well calibrated to a certain accuracy. Therefore, due to the lack of accurate on-chip power meter, factory calibration of at least one power level maybe needed
- In order to prevent doing factory cal for all Tx power levels (expensive), a Transmit-Signal Strength Indicator (TSSI) is designed to convert RF power to DC or low-frequency voltage. One factory cal is done at one power level, if the TSSI output voltage slope is constant over Tx power, if the TSSI slope is also calibrated (two points), then absolute power levels will be known for all Tx output power

Voltage sensing vs true power sensing for TSSI:

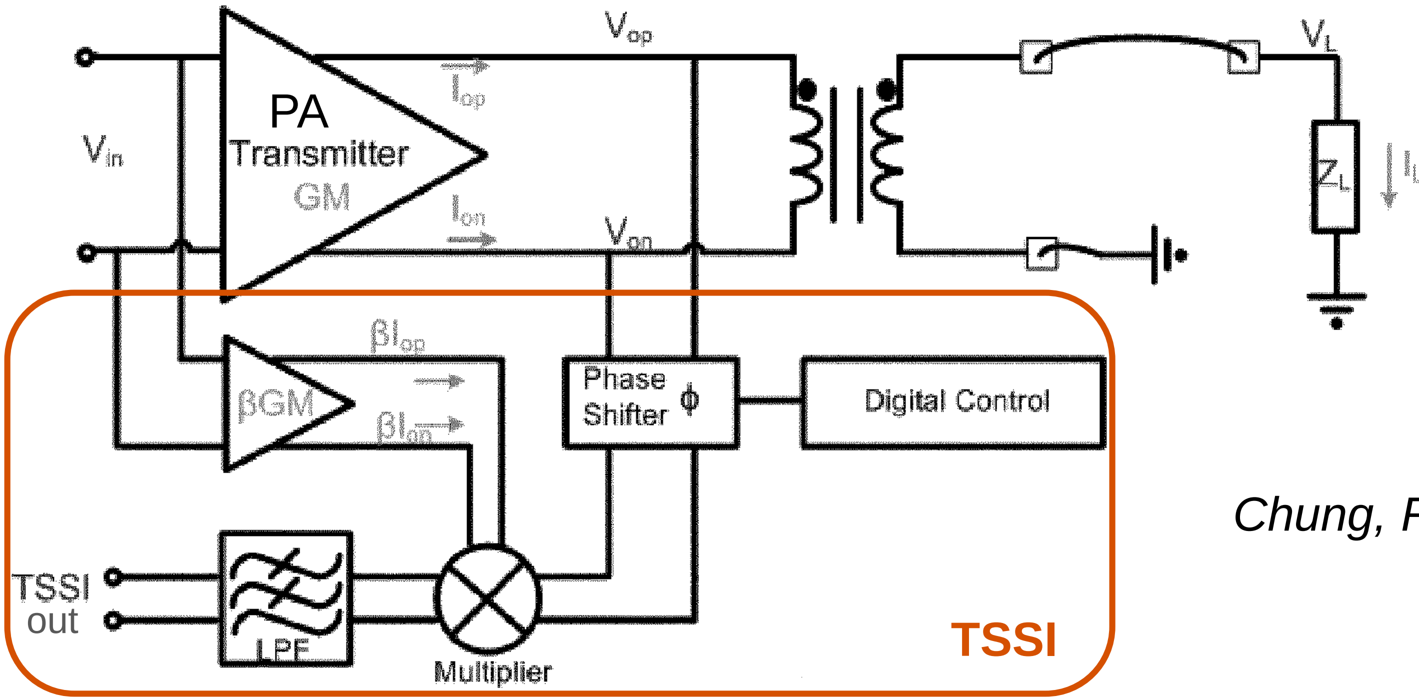


P_load = |V_load| x |I_load| x cosθ

- To properly measure output power, you need to measure it at the 50-ohm load (antenna) and not some internal node on-chip. In other words, you need to measure/sense V_load and I_load and calculate power from that (not easy to access the true load terminals).
- Sensing voltage schemes for TSSI has large error because the load current is missing. Also the scheme is sensitive to VSWR. However, this scheme is the easiest to implement and with some calibrations it can be made to work
- Power sensing schemes work best (for example RF coupler on PCB)

Pseudo power sensing for TSSI:

Replica load current x load voltage

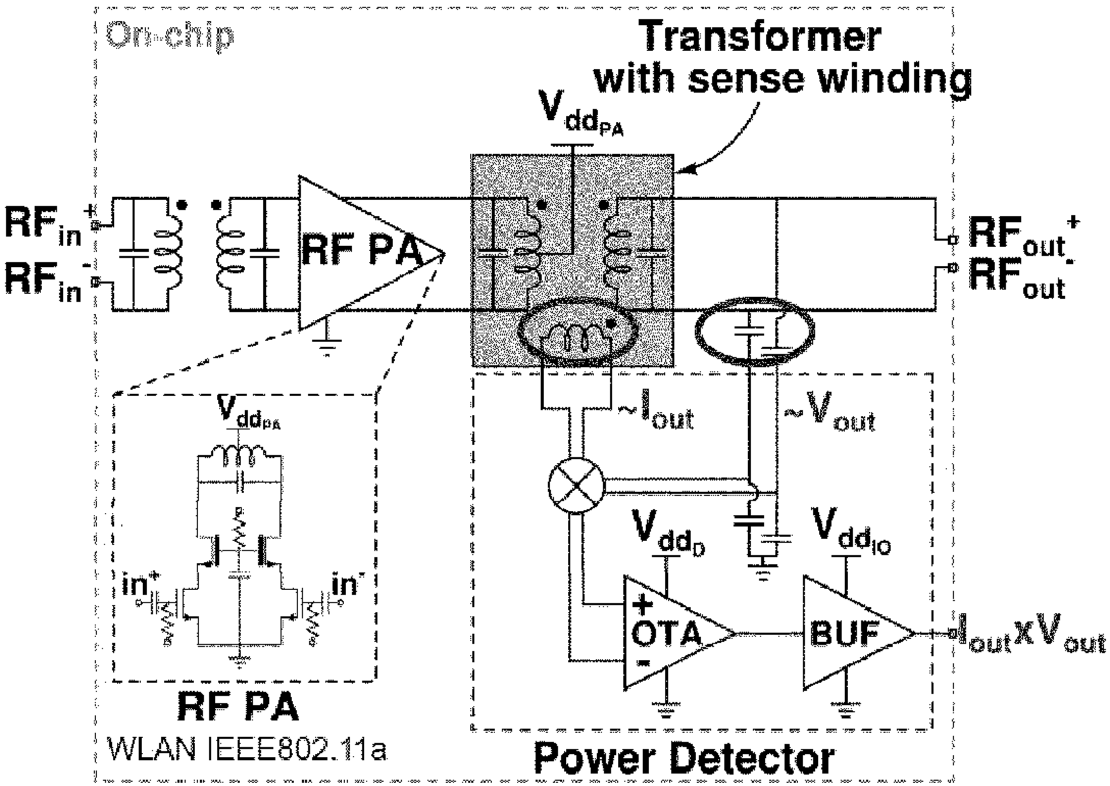


Chung, RFIC 2015

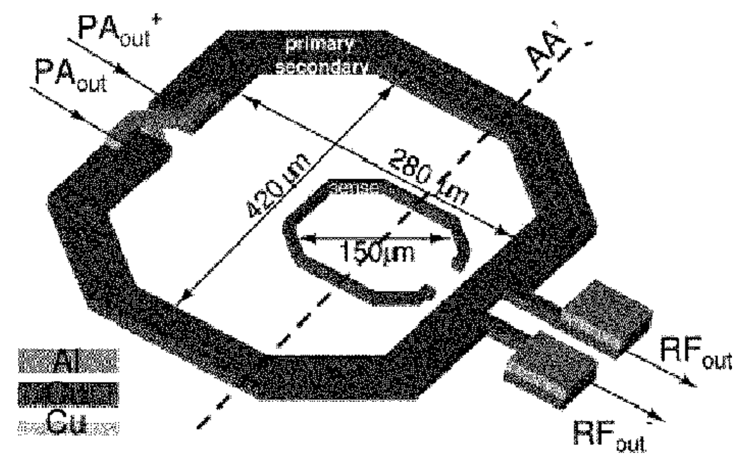
- Replica PA GM circuit (same GM as that of PA) is used to replicate PA load current. Load voltage is sensed at PA output (primary or secondary side of the balun is ok)
- During TSSI calibration, a 50-ohm load is used and the phase shifter is adjusted to get the maximum TSSI voltage output (the case for a pure resistive load). This takes care of finite I/V phase due to balun, package, PCB, etc.
- TSSI accuracy over 1:2 VSWR is +0.9dB/-0.6dB

Voltage sensing vs true power sensing for TSSI:

load current x load voltage



Francois, ISSCC 2014



- A small loop third coil is placed inside the PA balun to sense load current
- Sensing current depends on both primary and secondary coil currents (not just secondary) → sensing is till not perfect
- Error is not that much better than previous scheme over VSWR

References:

[1] C. Jones, et al., “Direct-conversion WCDMA transmitter with -163dBc/Hz noise at 190MHz offset”, *ISSCC Digest Tech. Papers*, pp. 336-337, Feb. 2007.

[2] X. He, J. van Sinderen, “A 45nm low-power SAW-less WCDMA transmit modulator using direct quadrature voltage modulation”, *ISSCC Digest Tech. Papers*, pp. 120-121, Feb. 2009.

[3] X. He, J. van Sinderen, R. Rutten, “A 45nm WCDMA transmitter using direct quadrature voltage modulator with high oversampling digital front-end”, *ISSCC Digest Tech. Papers*, pp. 62-63, Feb. 2010.

[4] F. Francois, *et. al*., "A transformer-Coupled True-RMS Power Detector in 40nm CMOS", *ISSCC Digest Tech. Papers*, pages 62–63, February 2014

[5] Y.-H. Chung *et. al*., “Dual-band Integrated Wi-Fi PAs with Load-Line Adjustment and Phase Compensated Power Detector”, *IEEE RFIC*, pp. 223-226, May 2015