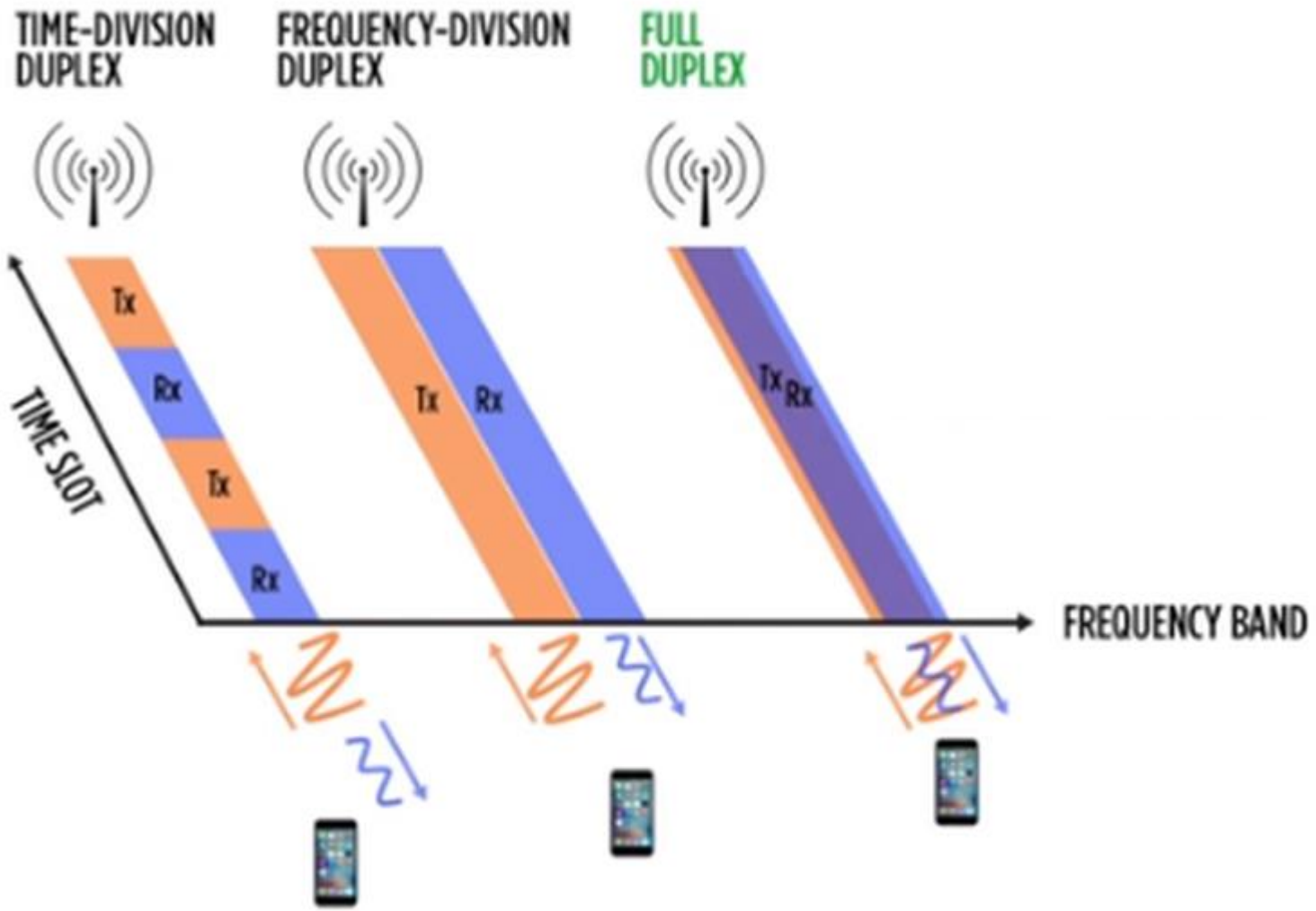
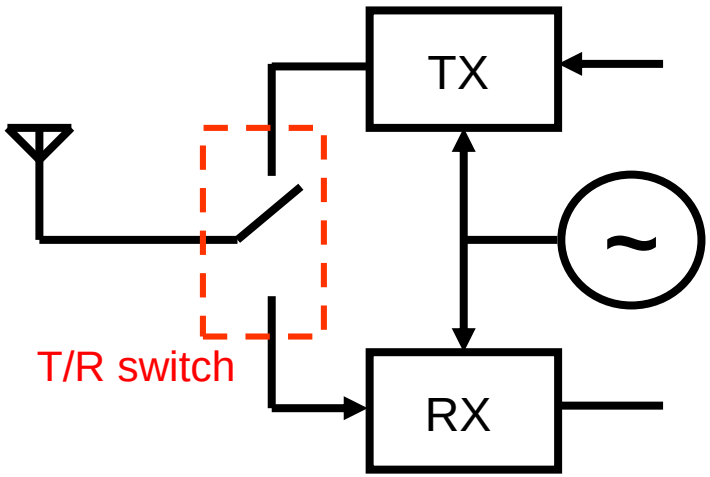
T/R switch design

- TDD system and the need of T/R switch
- Challenges of a T/R switch
- Active symmetric and asymmetric T/R switch
- Passive T/R switch
- References

FDD, TDD and FD Wireless system:

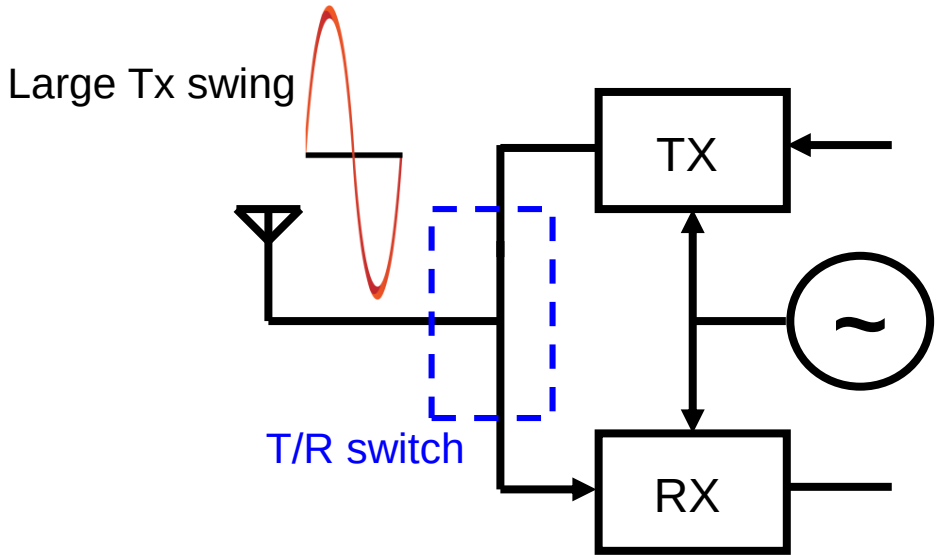


Time Division Duplex, TDD, Wireless system:



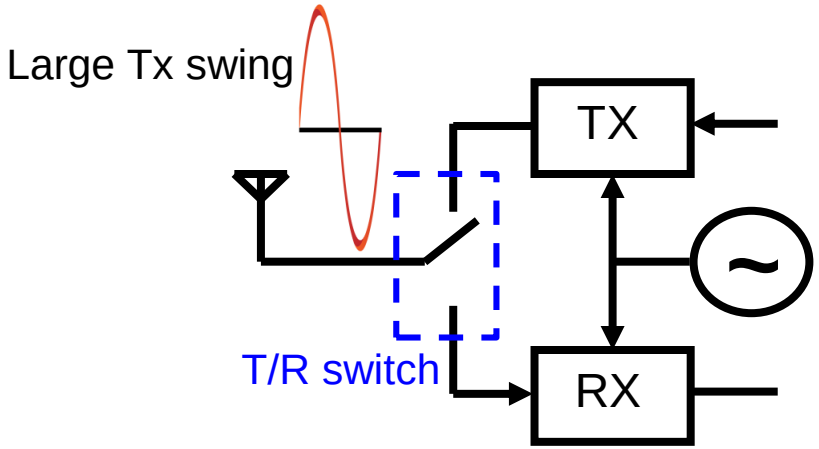
- In TDD system, both Tx and Rx share the same antenna via a T/R switch. They also share the same RF band, so they alternate in time (Time Division) with either Tx is ON and is connected to antenna, or Rx is ON and is connected to antenna (but not both ON at the same time during normal operation).

Why can't Tx and Rx share antenna without T/R switch?



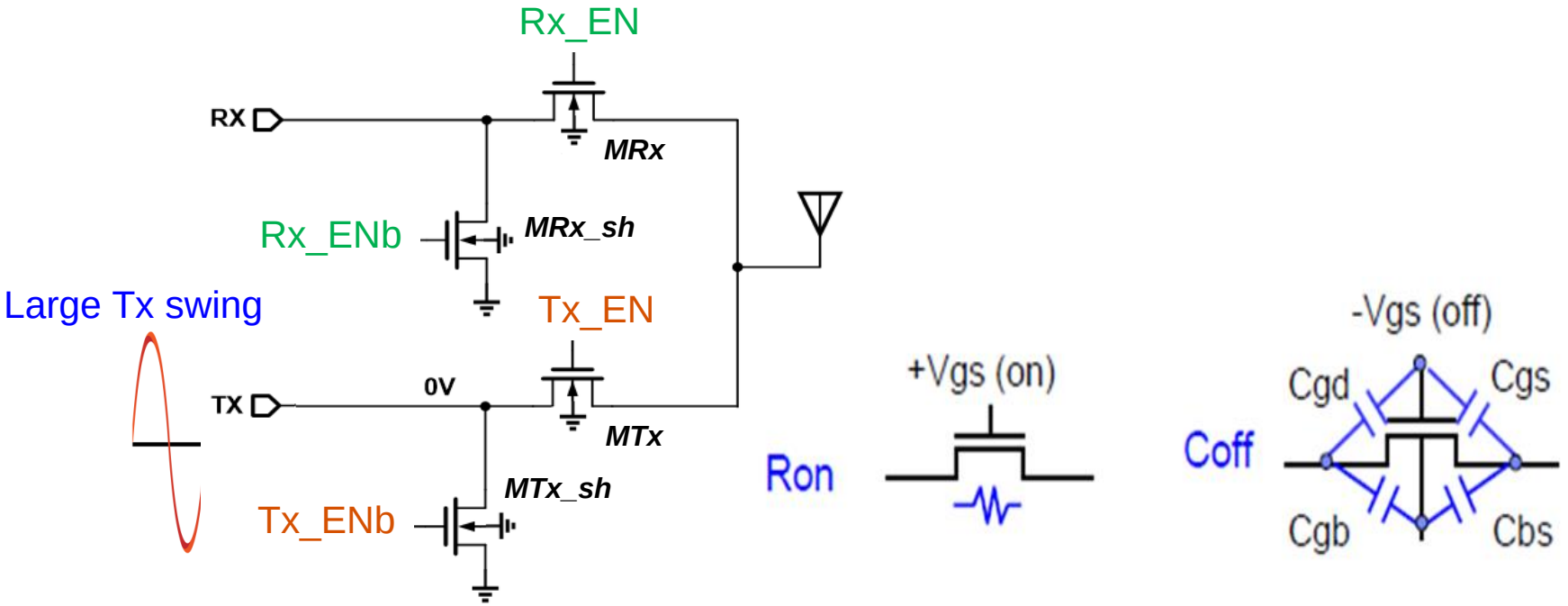
- Tx swing at antenna port can be quite large (~7V rms at 30dBm in 50Ω). With LNA (OFF) connected directly to Tx port it will experience device stress and device damage.
- LNA (OFF) can dynamically turn on/off due to large Tx signal resulting in possible AM-AM/PM degradation of Tx signal and possible memory effects
- LNA matching network connected to antenna can impact optimum PA load line degrading its Pout and efficiency
- PA (OFF) connected to LNA port can impact both NF due to loss in large PA device parasitic caps. It can also severely degrade LNA S11 and possible stability

Important specs of T/R switch in TDD transceiver:



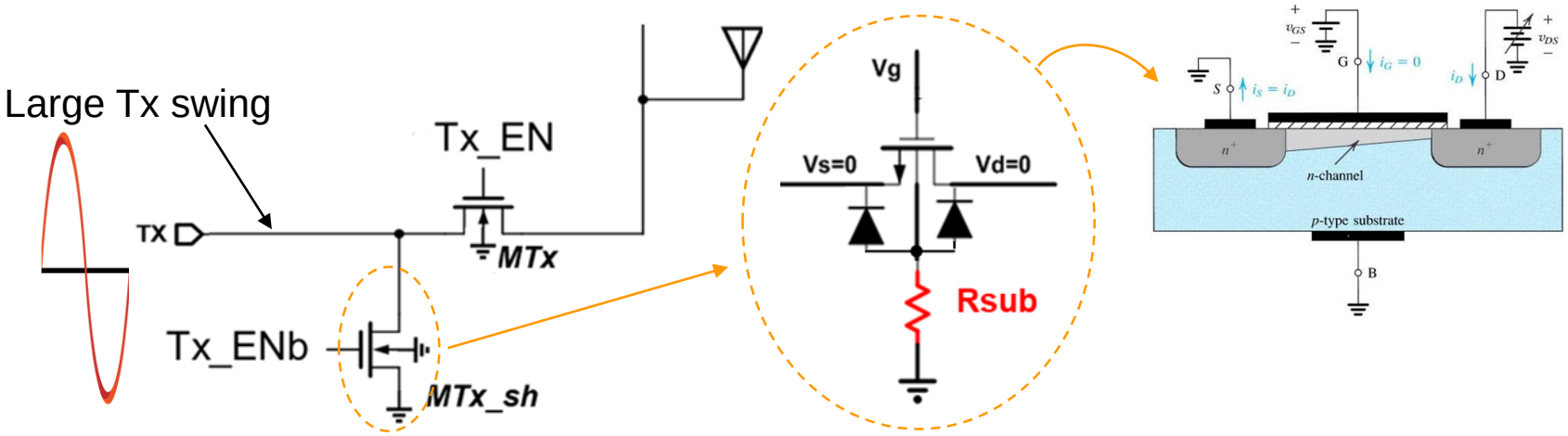
- **Insertion loss** in both Tx and Rx modes. Of course target is to have insertion loss as small as possible (<<1dB if possible). If loss is same in both Tx an Rx the switch is called symmetric. If the switch design favors one mode over the other, it is then called an asymmetric switch.
- **Isolation** between Tx and Rx ports. In TDD system the isolation requirement is relaxed (20~30dB because Tx is off when Rx is on and visa versa). The isolation is need to make sure Tx and Rx do not load each other (so not to impact S11, NF, Tx efficiency, etc) and also protect LNA from large Tx swing
- **Linearity**. The T/R switch P1dB has to be 6~10dB higher than that of integrated PA. So for a 30dBm P1dB for PA, the switch needs to have ~+36dBm (4W) of P1dB. Also IM3/IM5 of switch should be ~15dB lower than that of PA.
- **Reliability**. The switch has to be able to reliably handle Tx large swing. It also has to pass ESD requirement because it is connected to the antenna port

Device-based T/R switch: generic topology



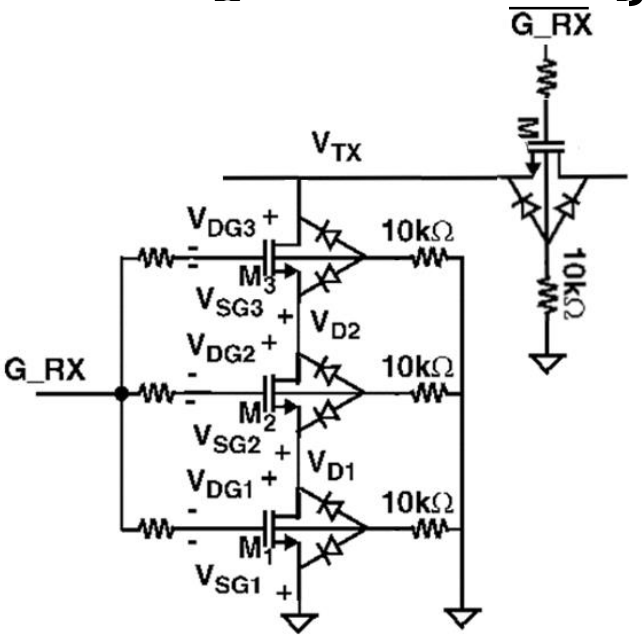
- MRx (and MTx) ON resistance is important for loss and its OFF capacitance is important for isolation → Ron x Coff is an important metric in device used for switch design. Ron x Coff ranges from 50fs~300fs depending on technology and layout
- MRx and MTx_sh are OPEN during Tx mode and so need to handle the large Tx swing (most prone devices to stress)
- MRx_sh is there to further protect Rx from Tx swing and is relatively easy to design (usually the smallest in size of all devices in the T/R switch). MTx_sh is to isolate the large OFF PA from Rx LNA during Rx mode so as it does not impact NF

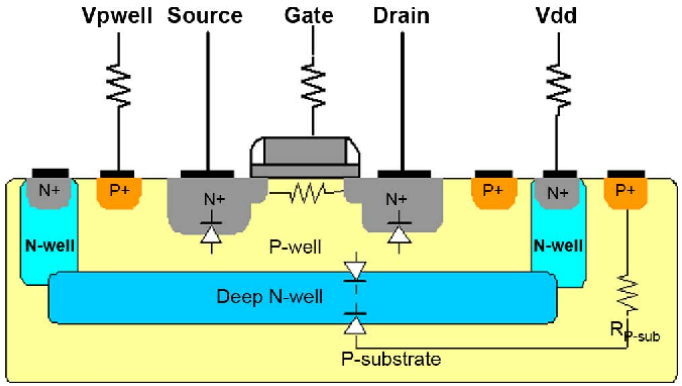
Can a normal bulk nmos handle-large swing?



- When Tx is enabled, MTx_sh is off (its gate DC voltage, Vgs =0). MTx is ON.
- The Tx port DC voltage is 0V (usually because of PA balun secondary winding to ground). This sets the drain voltage, Vd, of MTx_sh to also 0V
- During positive cycle of Tx swing, the OFF MTx_sh needs to handle this large swing at its drain (NCS reliability issue). Also MTx Vgs dynamically reduces causing severe distortion and loss.
- During negative cycle of Tx swing, the drain of MTx_sh swings below its gate causing device to dynamically turn on → bad distortion
- Similarly, because the substrate is also at 0V potential, the parasitic drain-bulk diffusion diode turns on during negative cycle of swing causing distortion
- Both devices experience high gate-source voltage under Tx swing (possible oxide break down)

Device stacking to handle large swing: use Deep-NWell

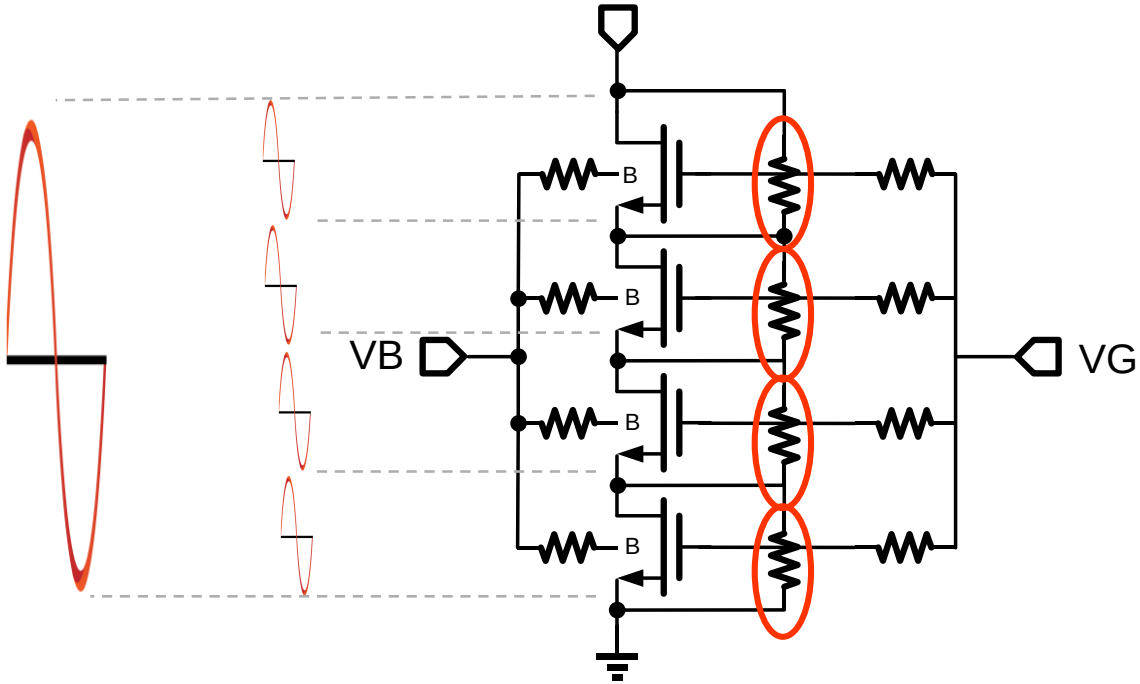




nmos in DNWL

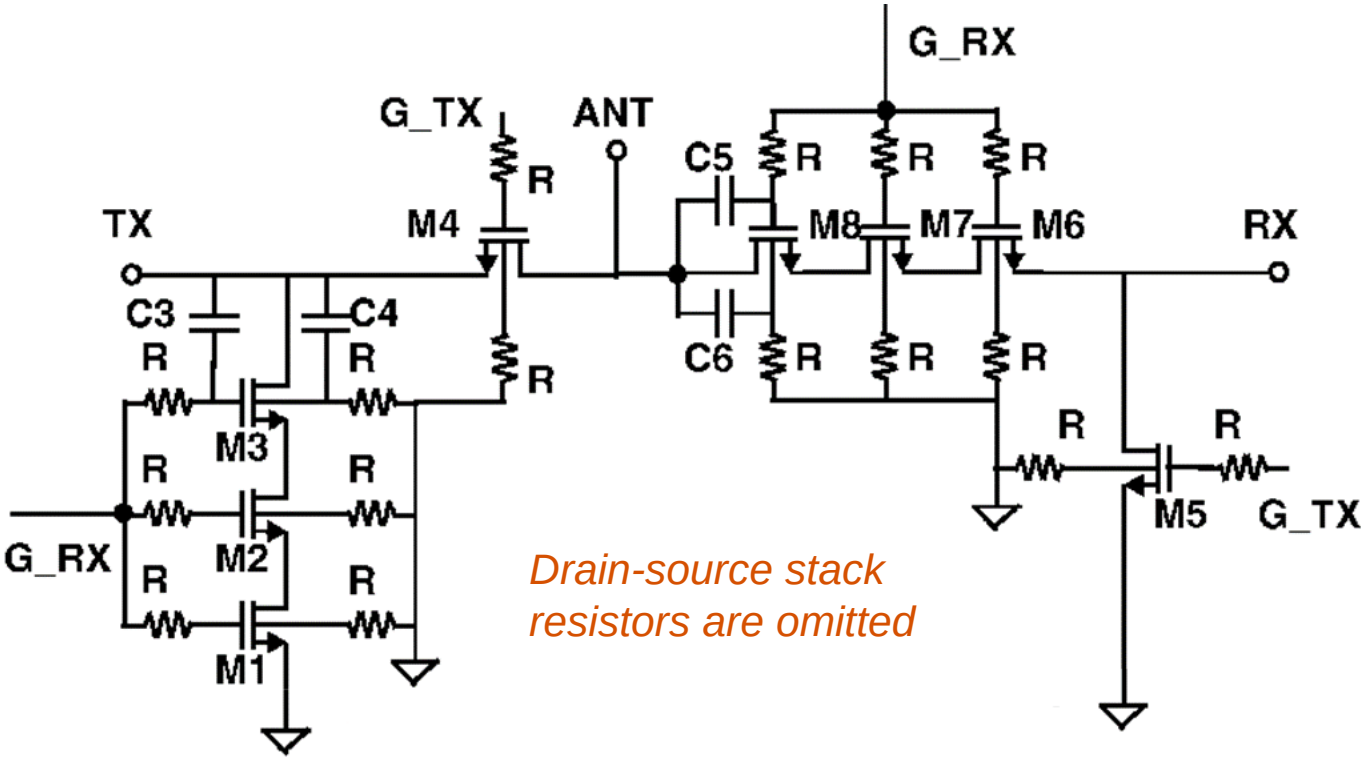
- NCS rating of a given technology is few volts and may not be enough to handle the large Tx swing especially under VSWR → one device will for sure breakdown
- The problem is solved by:
  - Stacking multiple devices so Tx swing is evenly distributed across the stack devices' Vds
  - Floating gate and bulk by adding a large resistance in series with the device gate (and bulk using DNWL device). This makes the signal at drain to couple to gate (and bulk) keeping Vgs and (Vdb) almost constant. This prevents the device (or diffusion diodes) from dynamically tuning on.

Proper even distribution of swing across stack:



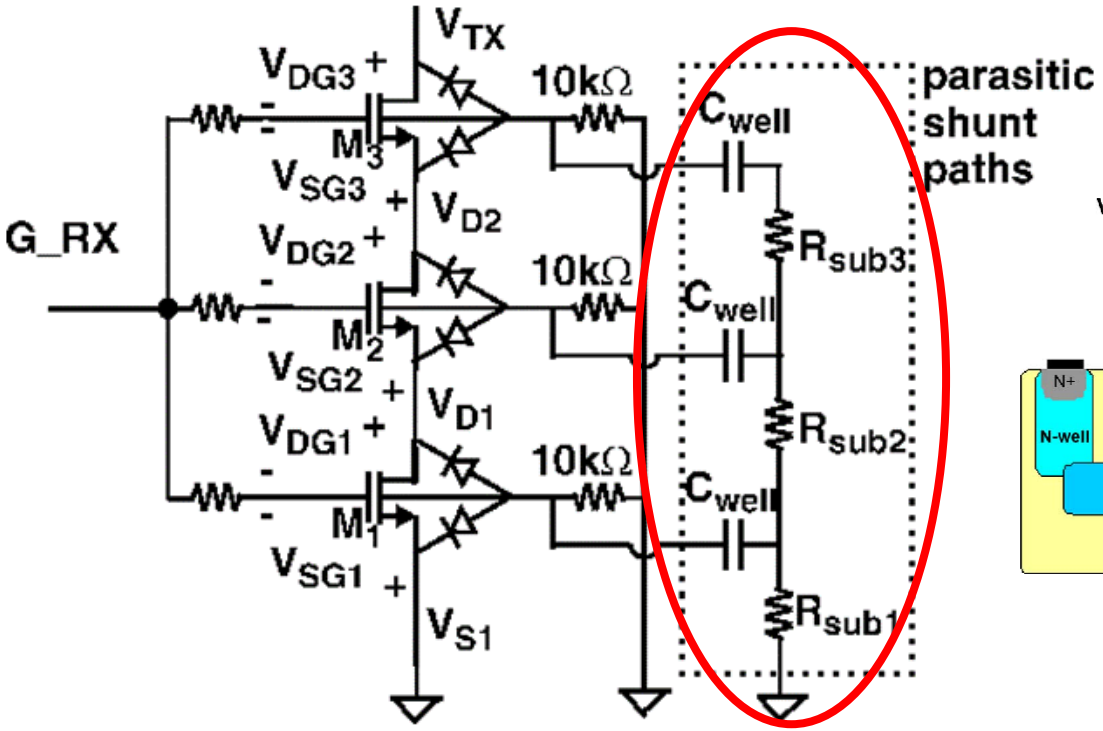
- When switch devices are off, drain-source voltage distribution in stack switch devices is sensitive to matching of OFF resistance of these devices (hard to control, especially with layout parasitics). As a result, one device in the stack may handle larger swing than other devices in the same stack causing reliability concern.
- A better way is to connect a large resistor (~10k) between drain& source terminals of each device in the stack. The voltage swing distribution is now set by the resistor stack rather by device impedance matching in OFF mode.

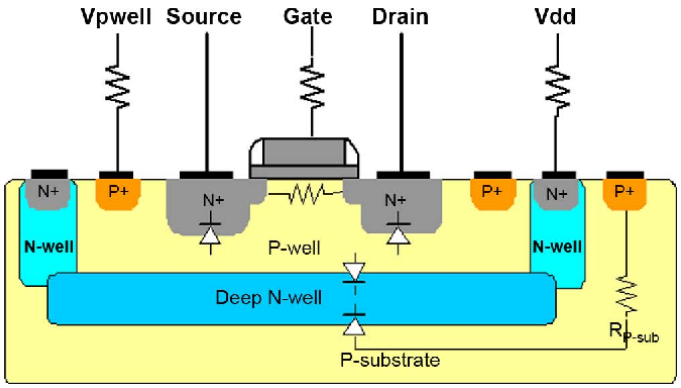
A complete T/R switch schematic:



- C3/C5 and C4/C6 are added to further couple AC signal to gate and bulk, respectively
- Deep N-well is needed for such design in bulk CMOS
- The drain of M4 and M8 need to be laid out in a way to pass ESD. Sometimes, an RF choke to GND at the ANT port maybe needed to further improve ESD at the expense of slightly degrading PA P1dB and LNA NF.

Sensitivity of switch loss to substrate resistance:

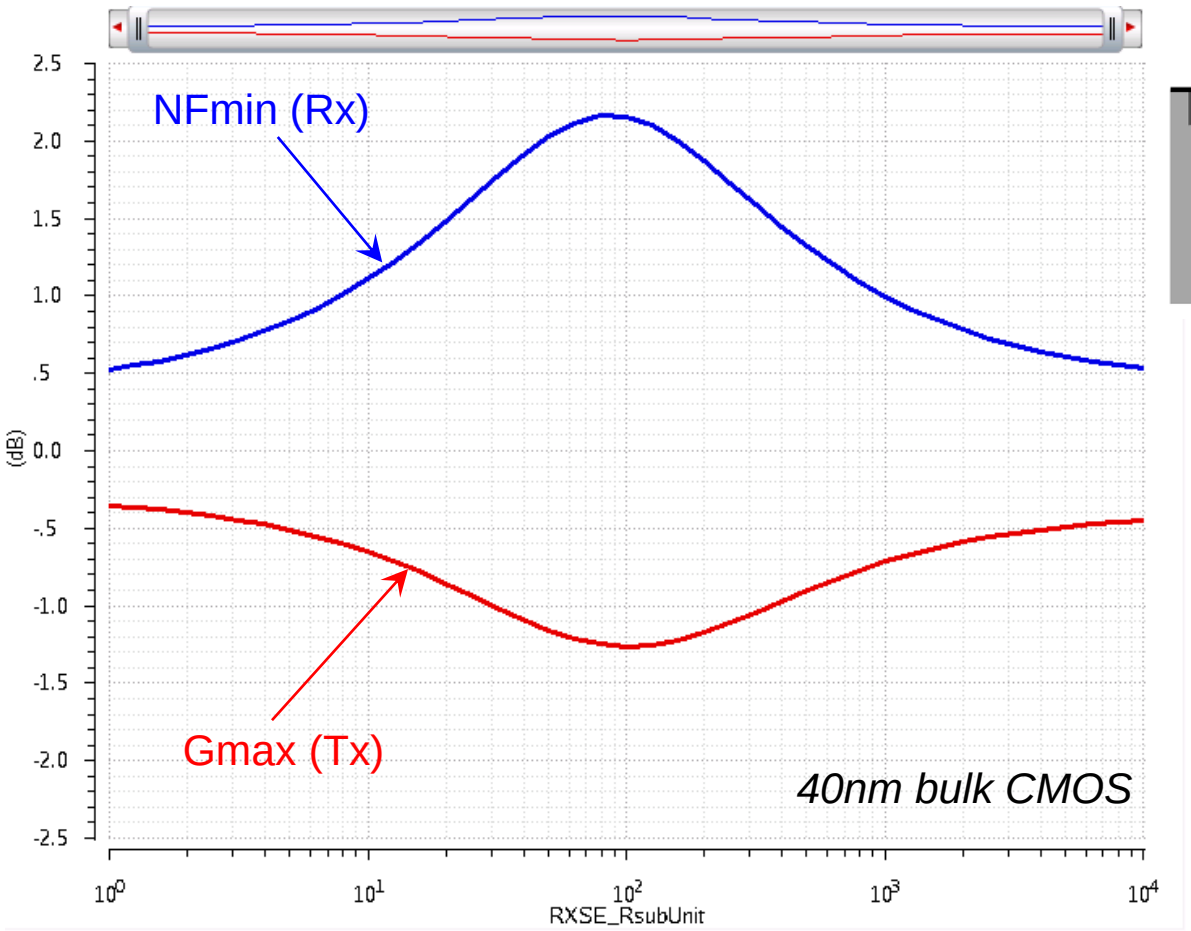


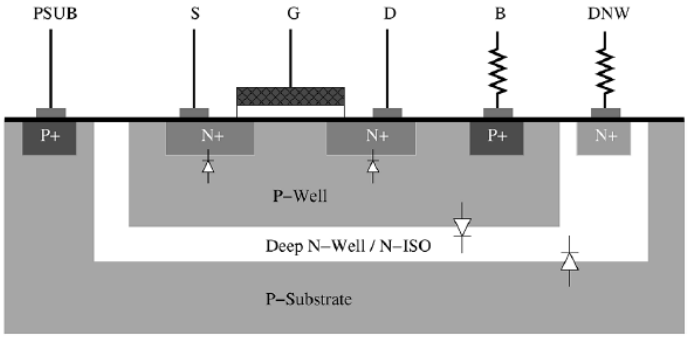


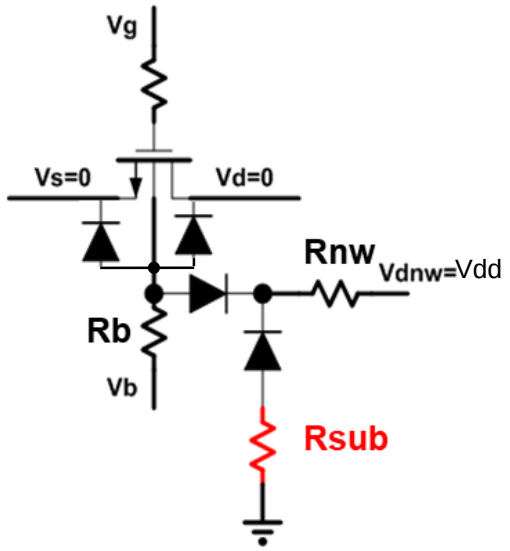
nmos in DNWL

- The drain diffusion diode of the stack switches is connected to the lossy p/nwell which in turn is capacitively coupled to the lossy p-substrate. This forms a lossy capacitive path degrading the switch loss
- The impact of this effect gets worse at high frequency. E.g, in 40nm CMOS, the loss of such switch is 1~1.5dB for WiFi 2.5GHz but degrades to 2.0~2.5dB at 5.5GHz band.
- It is quite difficult to model the substrate loss of the device for more accurate simulation (hard to correlate simulation with measurement)

Simulation of T/R switch loss vs substrate resistivity:

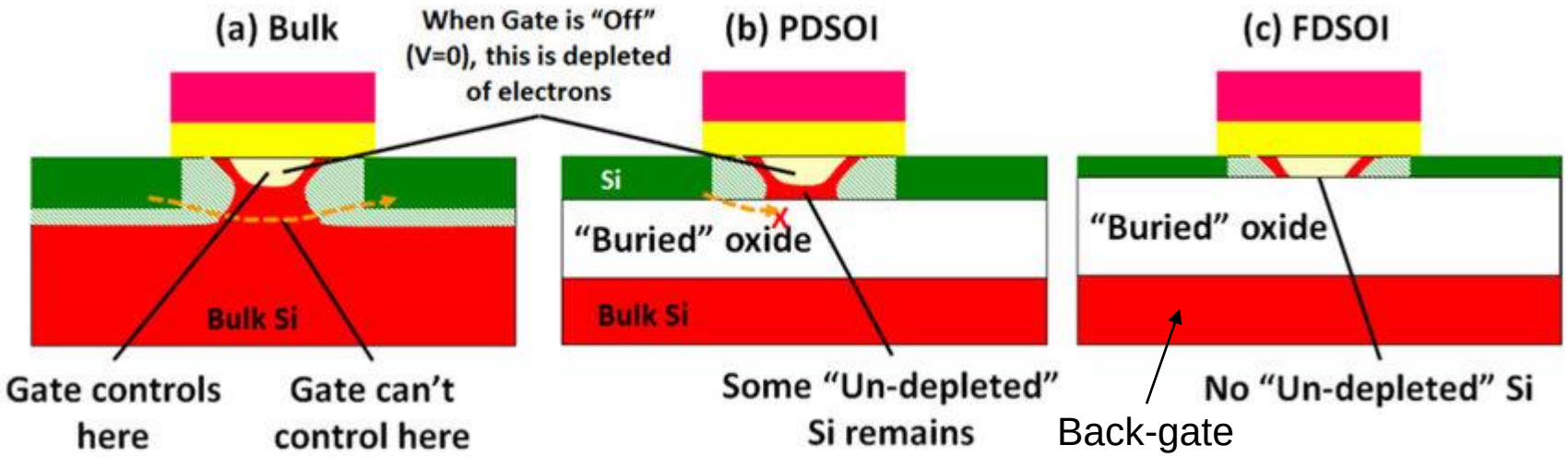






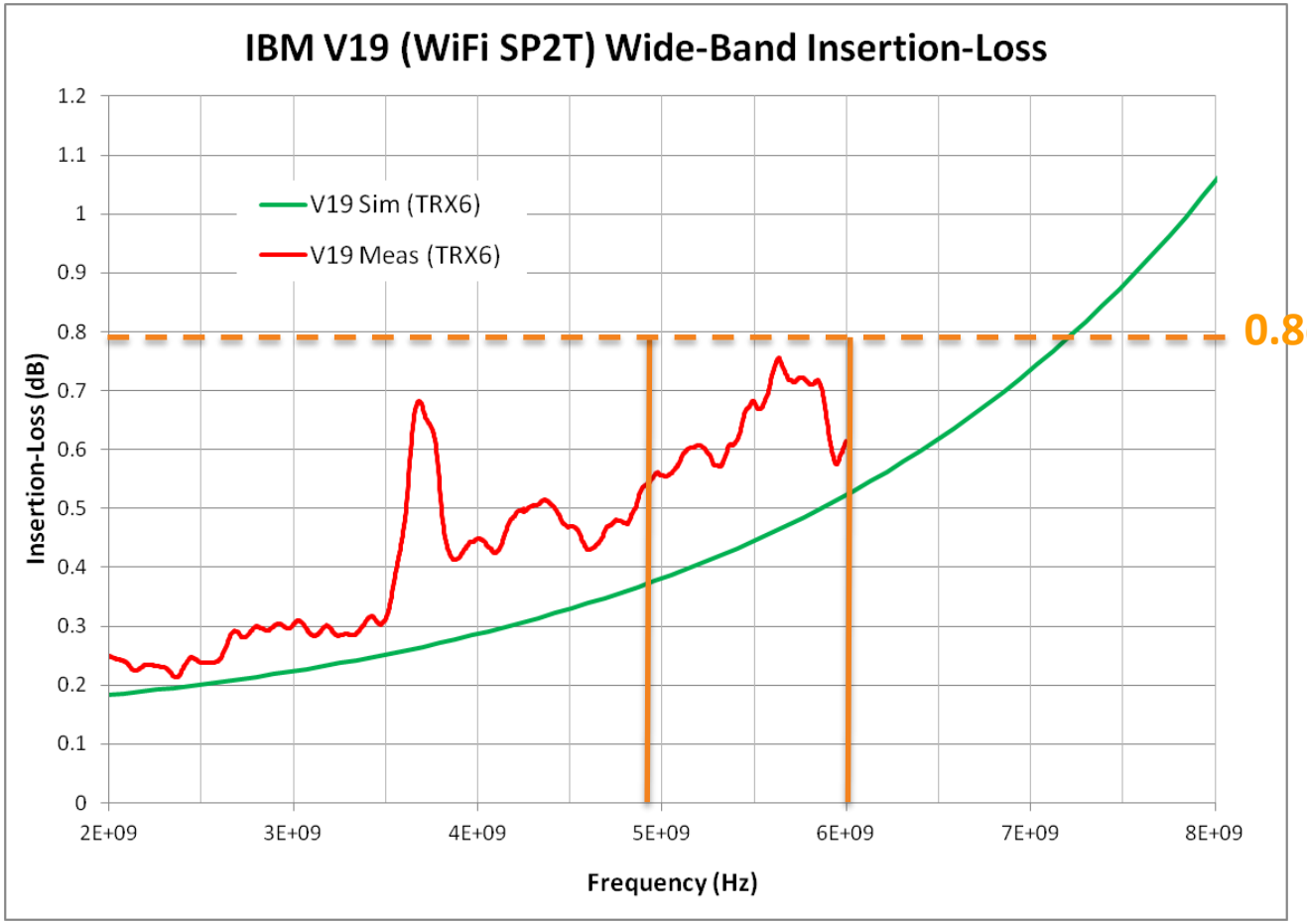
- As seen, performance is dependent on how well the switch Rsub is modeled.
- The plot also shows that for a high-resistivity substrate, the switch loss is at a minimum → **SOI CMOS** is the preferred choice for T/R switch design

Silicon on Insulator (SOI) CMOS process:



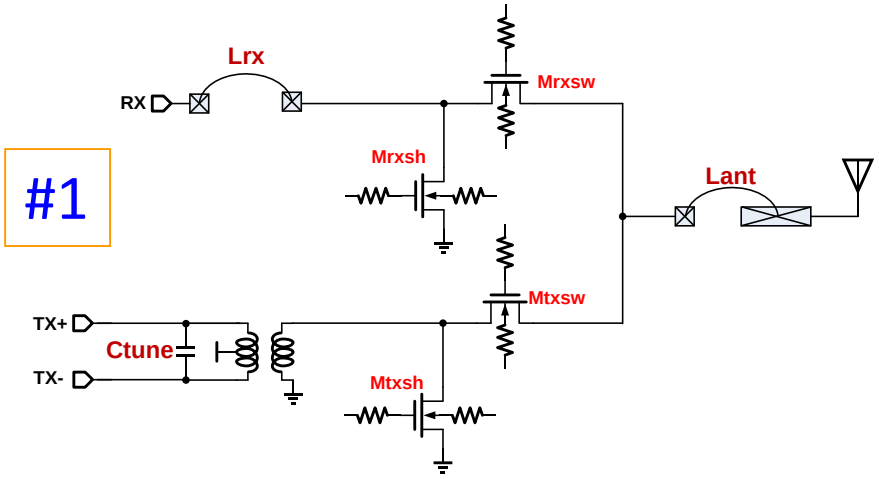
- The buried oxide, BOX, (thick oxide layer in the range of 0.1~0.2µm) isolates the device from the SOI substrate, which has resistivity near ~1kΩ.cm→ no bulk effect.
- Partially Depleted PD-SOI performance improves with floating body but has some side effects such as device hysteresis (memory) and kink effect. Fully Depleted FD-SOI solved these issues due to a much thinner body.
- In FD-SOI, Back-gate biasing (the other side of the buried-oxide) can be used to manipulate the device Vth.
- Negative bias sometimes is used to bias gate of OFF devices to further enhance linearity (generated by on-chip charge-pump-based design with a ring-oscillator clock <1MHz)
- As seen, no bulk for D/S diodes to turn on. Also thick BOX and high-res substrate highly reduce the impact of substrate on switch loss.

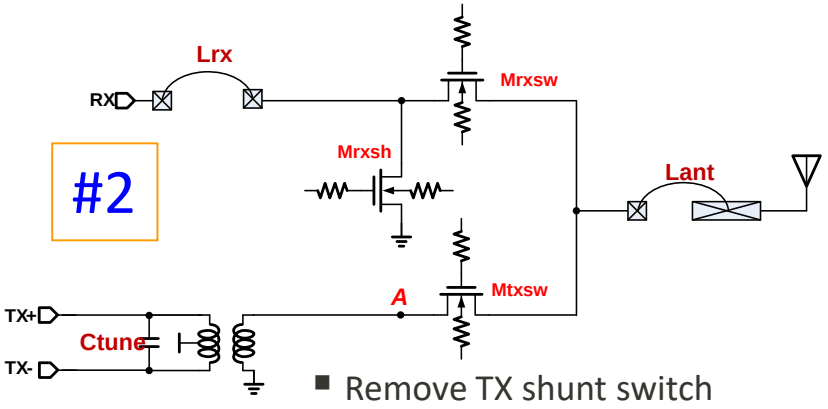
IL of T/R Switch in IBM's 0.18u PD-SOI (QFN pkg):

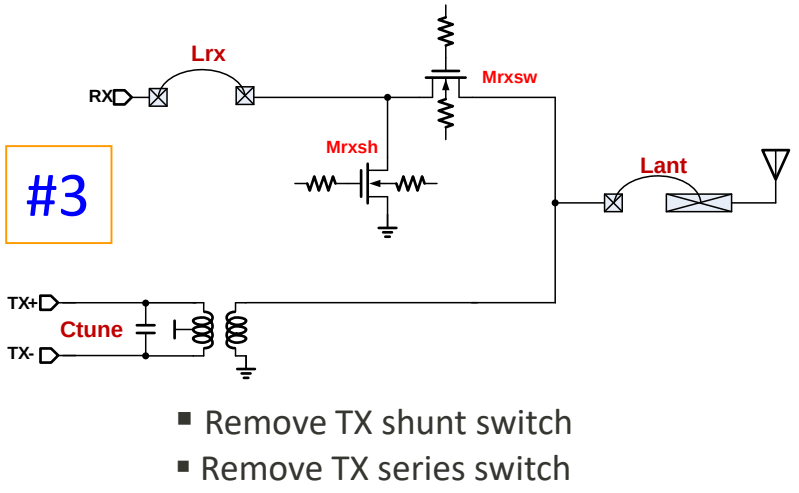


- Remarkable insertion loss of 0.55dB is achieved at WiFi 5GHz. The switch is designed for broadband RF. If it is optimized for 5.5GHz, a better IL can be achieved. This switch has P1dB>+35dBm

Asymmetric T/R switch:

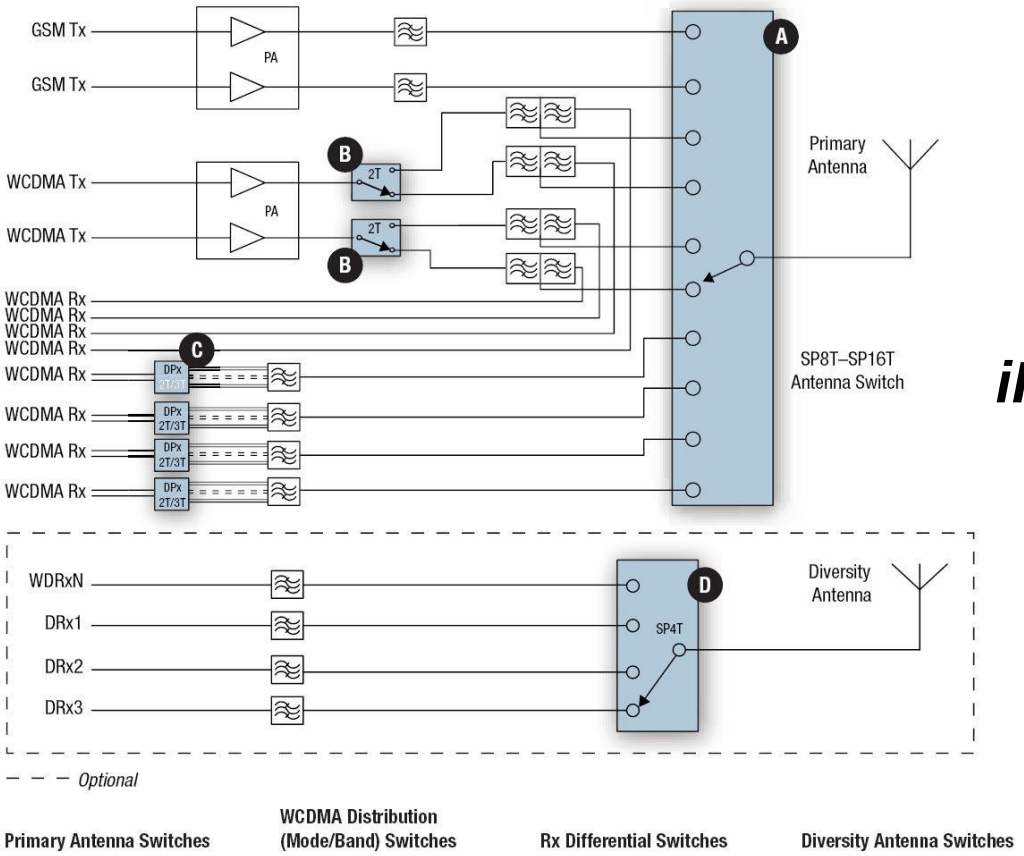






- In many systems, sometimes it is preferred to “favor” Tx over Rx in terms of switch loss. In other words, improve Tx mode IL of switch at the expense of degraded Rx mode IL and/or degraded isolation.
- A 0.5dB improvement in the IL of the switch in Tx mode improves PA efficiency by ~10% (so if efficiency of PA + original switch is say 9%, the efficiency of PA + improved switch becomes ~9.9%). T/R switch #2,3 favor Tx

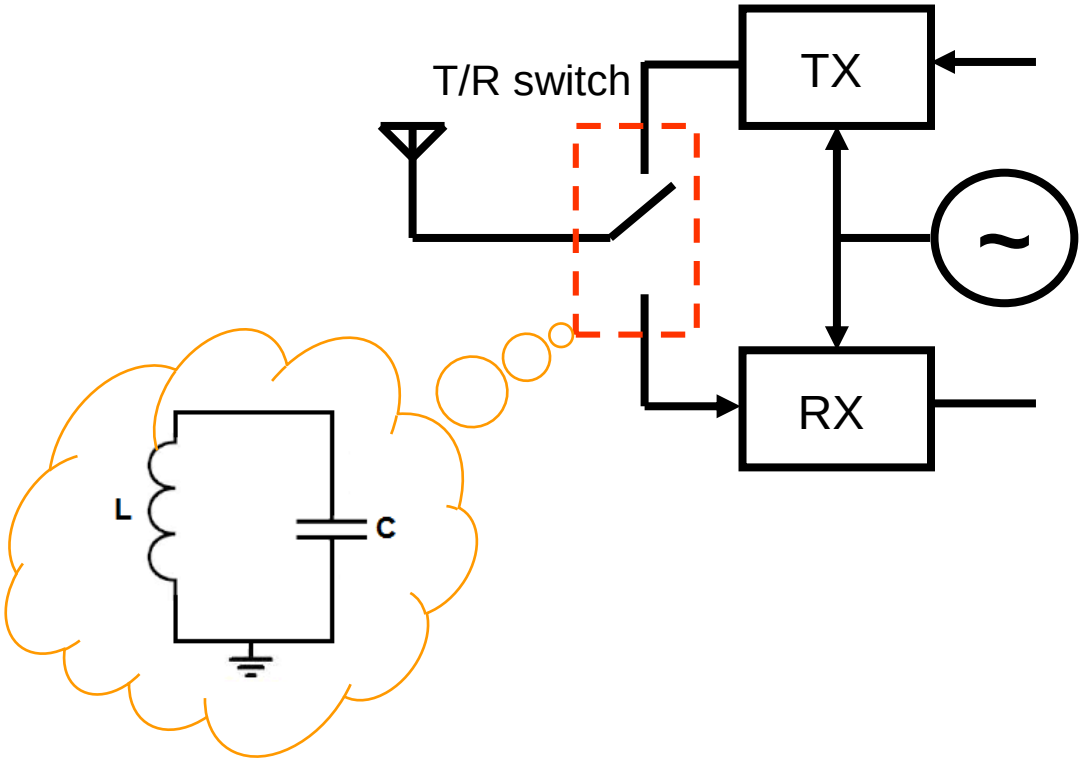
SOI RF switches are in high-demand:



iPhone 5

- Cellular transceivers are getting complicated due to so many bands of 2G/3G/4G/5G sharing same antenna → a single-pole N-throw switch is needed to interface the so many transceivers with a single antenna
- RF Switches contribute nearly half of annual revenues of some FEM companies!

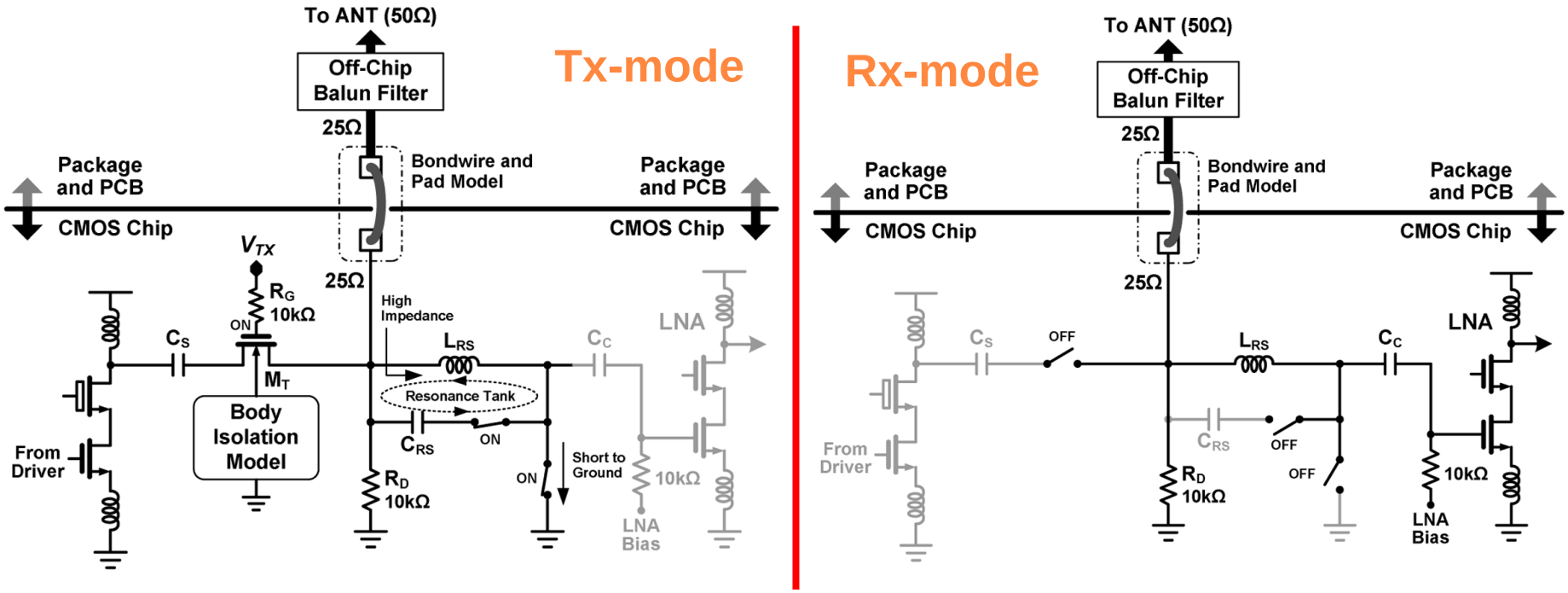
Passive T/R switch:



- Because of the complications of using a device as T/R switch (reliability, ESD, substrate loss, etc), a passive switch serves an alternative (especially if there is no access to exotic technology like SOI)
- The idea is to use resonance circuits configured by switches to ground (whose performance does not impact loss) between Tx and Rx modes.

Passive T/R switch:

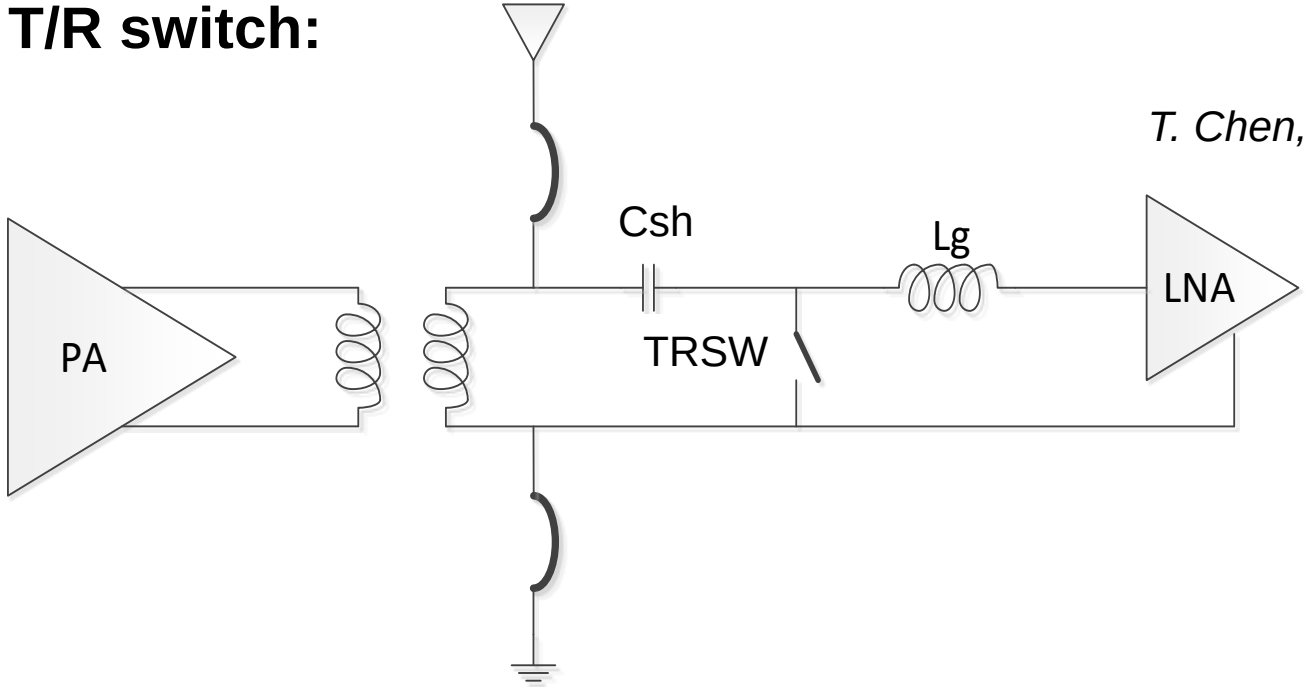
Kidawi, JSSC 2009



- A C_{RS} cap in series with a switch forms a parallel resonance at RF isolating LNA from large Tx power. No switches need to handle any large swing → no sensitivity to substrate loss
- Design is sensitive to resonance centering
- At 2.5GHz, Insertion loss <0.4dB is achieved. Isolation is >16dB (normal bulk CMOS)

Passive T/R switch:

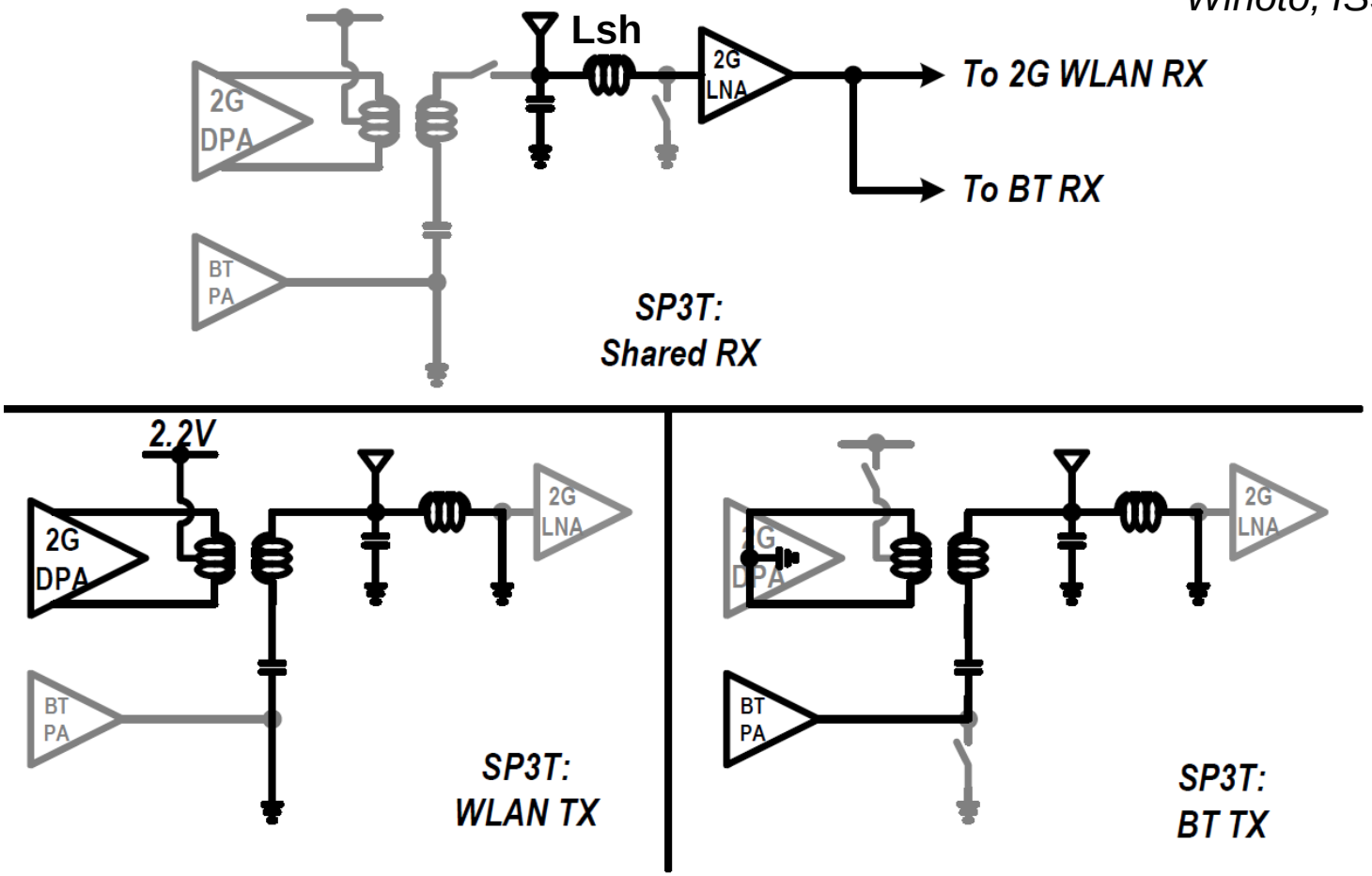
T. Chen, RFIC 2014



- In Tx mode, TRSW is short to ground, protecting LNA from large Tx swing. In this case, Csh forms a parallel resonance with balun secondary for PA output matching. In Rx mode, the TRSW is open, Csh becomes an AC coupling cap for LNA.
- This T/R switch favors the transmitter (loss in Tx mode is <0.3dB at 5GHz). However, in Rx mode, LNA sees the large parasitic loading of PA (OFF) causing NF (and S11) degradation. Loss in Rx mode is ~1dB.
- No ESD concern due to PA balun secondary to ground at antenna port.
- Tx/Rx co-matching is tedious due to shared Csh between Tx and Rx.

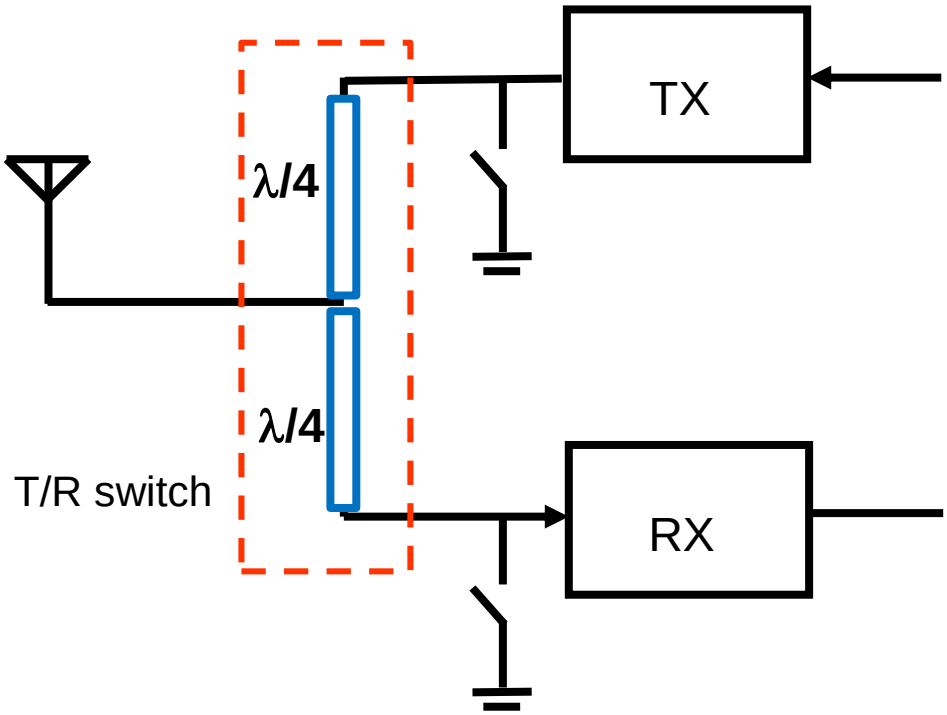
Passive T/R switch:

Winoto, ISSCC 2016



- Same as Chen's switch except replace Csh with inductor Lsh.
- Design is sensitive to the Q of Lsh. Insertion loss of Tx can be as large as 1dB but loss in Rx mode is better than Chen's (~0.8dB better)

mmWave λ/4 T/R switch:



- Conventional T/R switch for mmWave uses λ/4 TL to isolate Tx from Rx
- Since is quite large for 5G mmWave (28GHz) to integrate (done on PCB).
- Loss is set by the TL loss and how perfect the switch short is.
- There are derivatives of this as well that combines TL and switches

References:

[1] Adil Kidawi, *et. al.*, “A Fully Integrated Ultra-Low Insertion Loss T/R Switch for 802.11b/g/n Application in 90 nm CMOS Process,” IEEE JSSC, Vol.44 No.5, May 2009, pp 1352-1360.

[2] T. Chen, et al, “A 2x2 MIMO 802.11 abgn/ac WLAN SoC with integrated T/R switch and on-chip PA delivering VHT80 256QAM 17.5dBm in 55nm CMOS,” *IEEE Radio Frequency Integrated Circuits Symp.*, pp. 226-228, June 2014

[3] R. Winoto, et al, “A 2x2 WLAN and Bluetooth Combo SoC in 28nm CMOS with On-Chip WLAN Digital Power Amplifier, Integrated 2G/BT SP3T Switch and BT Pulling Cancellation,” *in conference proceedings ISSCC 2016.*

[4] Q. Li, *et. al.*, “CMOS T/R Switch Design: Towards Ultra-Wideband and High Frequency,” IEEE JSSC, Vol.42 No.3, March 2007, pp 563-572.

[5] Y.H. Lin, *et. al.*, “A 900-MHz 30-dBm Bulk CMOS Transmit/Receive Switch Using Stacking Architecture, High Substrate Isolation and RF Floated Body,” *Progress In Electromagnetics Research C, Vol. 11, 91-107, 2009*.

[6] H. Xu, *et. al.*, “A 31.3-dBm Bulk CMOS T/R Switch Using Stacked Transistors With Sub-Design-Rule Channel Length in Floated p-Wells,” IEEE JSSC, Vol.42 No.11, November 2007, pp 2528-2534.

[7] A. Madan, *et. al.*, “Fully Integrated Switch-LNA Front-End IC Design in CMOS: A Systematic Approach for WLAN,” IEEE JSSC, Vol.46 No.11, November 2007, pp 2613-2622.