EECS 290C: Advanced circuit design for wireless
Class Final Project
Due: Thu May/02/2019

Project: A fully integrated 2.4-2.5GHz Bluetooth receiver. The receiver has LNA, RF mixer, baseband complex filter, VCO and LOgen

Technology: T28nm CMOS (BWRC students), generic 45nm CMOS for others

Package: 28-pin QFN, with exposed paddle.

Logistics: a group of 3-4 students can take on the task to design the entire receiver as one team. Students within each group has to agree on who designs what (one block per student). It is encouraged that the team members meet on regular basis to discuss project progress.

Deliverables: a design-review-like package (or a JSSC-like paper format) needs to be submitted at the end of project deadline (each student submits his/her own design report). This includes:

- circuit description (with topology selection reasoning and derivations/calculations if any)
- a full set of annotated circuit schematics (showing component values, node bias voltages, branch DC currents etc)
- simulation plots clearly marked with comments
- a table showing side by side spec vs. simulation. Highlight the specs you missed in red font.
- a one page showing the layout floor plan of your design (where to place each component in the design relative to others using a drawing tool) and also place critical lines in the drawing (signal path, Vdd, gnd, etc). Use colors to make it easy to read
- The report should not exceed 20 pages max.

IC Architecture: low-IF architecture with dual IF frequency of 0.9/1.8MHz. The system calculations are omitted here but a procedure similar to that derived in class are applied here to derive the system specs as well as per-block specs

Goal: meet or beat target performance specifications at lowest current consumption. The block that meets the corresponding specs without exceeding the current consumption budget gets the highest grade. A Plus is given to designs with smallest area, lower current and novel design ideas.

Operating conditions:

- V_{dd}: 1.2V ±10%
- Ambient Temp: -20°C to +70°C
- Typical values are for 1.2V V_{dd} , 2.45GHz and 27°C.

Main system spec targets:

- I_{dd}: 7.5mA <10mW power consumption).
- NF: ~3dB typical at LNA input

- Max Av: 53dB
- AGC: 24dB range in 1dB steps (insufficient for actual BT receiver but good enough for a class project)
- OP1dB: >1Vpp
- V_{offset}: <100mV at I/Q baseband output
- IRR: >20dB

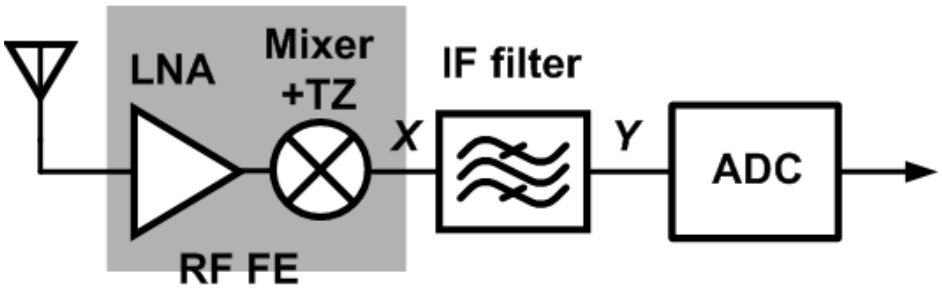
Important issues:

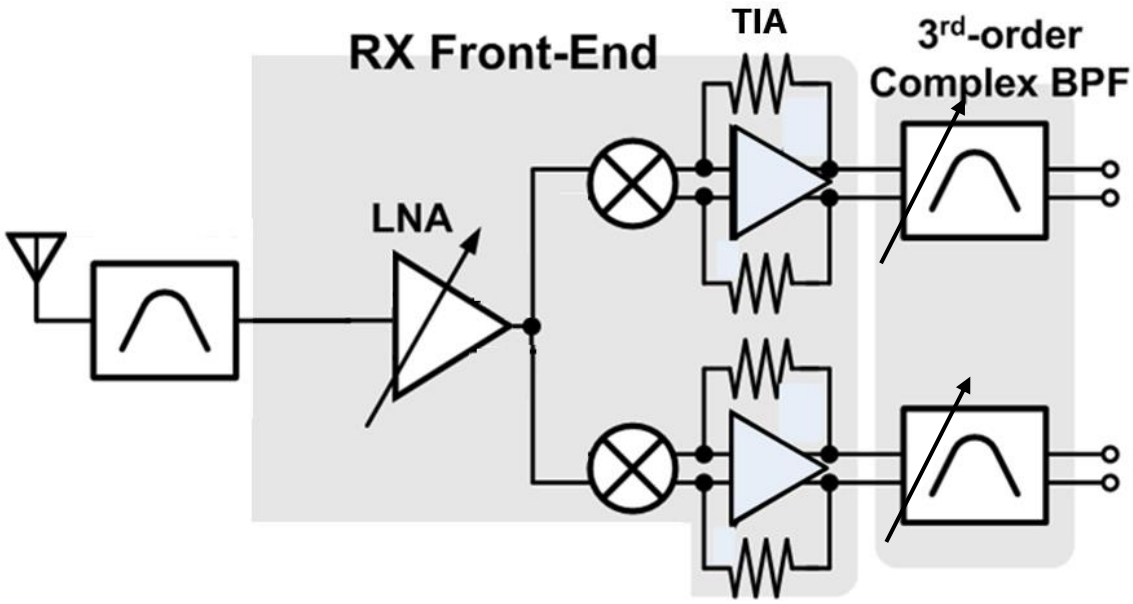
- Single-ended LNA for both input and output. LNA input is fully matched on-chip to 50Ω. LNA output drives mixer directly on-chip (no power matching needed)
- The I/Q mixer can be single-balanced. If you want to use a double-balanced topology you need to add a balun at mixer input with a loss of 1.5dB to interface with the single-ended LNA (the balun loss will count from your mixer NF/gain budget). You can use any active mixer topology you want (Gilbert-cell mixer, passive one followed by TIA, etc). The block diagram below assumes a single-balanced passive mixer with TIA. Mixer RF input is voltage driven (no power matching needed to LNA output). The RF input impedance to your mixer has to be high enough not to load the LNA to isolate mixer from LNA (use your experience from HW4 to get an idea how much unmatched LNA load impedance is to decide about your mixer Zin to be high enough not to impact LNA gain by more than 1dB). If you want to generate 25% LO for your mixer you need to design the circuit for that as the I/Q LO coming to you is 50% from a divide-by-2 circuit.
- For TIA and Complex Filter, you need to use an actual opamp circuit. I am okay to borrow the circuit from a previous design you have done in a separate class or use a topology from a text book. I am also OK if TIA and filter use same opamp circuit.
- Mixer output (TIA output if used) and complex filter in/out are all differential.
- Please do not use ideal components in your design. Use resistors, capacitors, etc. from PDK. Use actual bias voltage and current circuits to bias your block (no ideal biasing). For on-chip inductors, you can either use ones from PDK roster that is close to the value you need or use an inductor from analog lib and set Q to ~10 (you can assume Q is set by inductor wire series R just like in HW3). For Vdd you can assume an ideal voltage source at the package input on PCB. You also can assume an ideal 0.8V bandgap voltage source on chip with noise of 55nV/sqrt(Hz), see below.
- You must specify the bias flavor to your blocks (bandgap referenced over on-chip resistor, PTAT, constant-gm, etc.). You must also include bias noise (similar to that of HW4) in your sims.
- Any block can use down bonds to the paddle for additional grounds. The IC has a 3-wire Serial Bus Interface (SBI) for digital programming/control.
- VCO block design is optional as we did not cover the topic yet in class. However, I won't stop a student from trying to design one if he/she is familiar with the topic or wants to try it. Each group of 3 students should cover LNA, mixer/TIA, and CLPF design (mandatory) but VCO can be optional. A 4th student is needed if the group wants to cover VCO.

Milestone Time Table: the dates below are to help you organize your progress:

1. **End of 4/16/2019**: have your preliminary skeleton circuit design schematic done with circuit meeting all typical specs. You can use ideal resistors, capacitors and biasing at this stage while you are refining your circuit.
2. **End of 4/23/2019**: ideal components are replaced with real ones and real biasing is used. Re-check performance to make sure things did not change. At this stage you need to include package model in your design. Check PVT to ensure robustness of your design. If you miss few specs over PVT and you are short in time, it is okay as long as you highlight that in your report. Meeting performance over PVT is a plus, however I expect your design not to completely collapse under PVT.
3. **End of 4/30/2019**: all performance plots/numbers are generated for your design and your design report is pretty much complete
4. **5/(2&7)/2019**: presentation of your work

IC block diagram:





Block diagram of BT Low-IF RF receiver

Block spec details:

Min and Max numbers should be met over PVT. Typical values are for 1.2V V_{dd} and +27C temperature. Note that current consumptions spec should be only used as a guideline as a design target (you can exceed it if you have to).

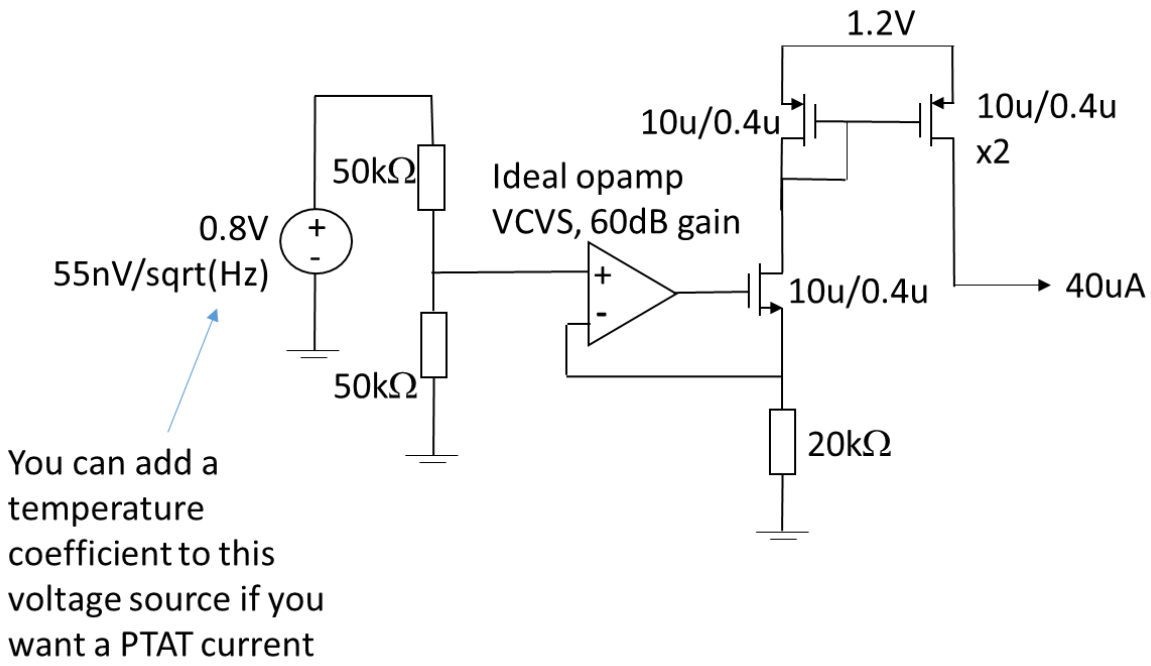
no	spec	condition	min	typ	max	unit
LNA						
1.1	Frequency	All modes	2400		2500	MHz
1.2	Supply Current	All modes			2	mA
1.3	Voltage Gain	High-Gain mode	18	20	22	dB
		Mid-Gain mode	12	14	16	
		Low-Gain mode	6	8	10	
		ultra-Low-Gain mode	0	2	4	
1.4	NF	High-Gain mode		2	3	dB
		Mid-Gain mode		3	4	
		Low-Gain mode		5.5	7	
		ultra-Low-Gain mode		9	11	
1.5	IIP3	High-Gain mode	-13	-10		dBm
		Mid-Gain mode	-7	-4		
		Low-Gain mode	-3	0		
		ultra-Low-Gain mode	-1	+2		
1.6	IP1dB	High-Gain mode	-23	-20		dBm
		Mid-Gain mode	-17	-14		
		Low-Gain mode	-13	-10		
		ultra-Low-Gain mode	-11	-8		
1.7	25MHz blocker IP1dB desense	Either in-band noise rise or gain loss by 1dB (all modes)	-27			dBm
1.8	Phase change	Gain switch between any gain modes		0°	8°	degrees
1.9	Input return loss, S11	All modes			-10	dB
1.10	gain switching time	between any gain modes			0.5	µs

no	spec	condition	min	typ	max	unit
Mixer (+TIA)						
2.1	Frequency	input RF	2400		2500	MHz
2.2	Low-IF center frequency	IF signal BW is 1MHz for BDR mode and 2MHz for EDR		0.9 1.8		MHz
2.3	Supply current	I + Q, includes LO buffers (and TIA)			3.5	mA
2.4	Voltage gain	RF in to I or Q output	13	15	17	dB
2.5	input referred noise	I or Q output noise referred to RF input voltage		5	6	nV/sqrt(Hz)
2.6	out-of-band IIP3	RF blockers 15, 29 MHz offset from LO. IM3 falls at 1MHz IF	-12	-9		dBVrms
2.7	out of band IIP2	RF blockers 25, 26 MHz offset from LO. IM2 falls at 1MHz IF	17			dBVrms
2.8	IIP3	two tones and IM3 all in-band	-12	-9		dBVrms
2.9	IP1dB	in-band input-referred rms voltage compression	-22	-19		dBVrms
2.10	Mixer pole frequency	Placed at IF	4	5	6	MHz
2.11	I/Q output DC common-mode voltage	I/Q output to interface with following LPF	550	600	650	mV
2.12	output DC offset	3-sigma. I and Q outputs			±12	mV
2.13	LO buffer guaranteed input swing	Input swing to I/Q LO buffers from divider. 50% duty cycle	300			mVpp
2.14	intrinsic image rejection (I&Q imbalance)	3-sigma of linear histogram (or worst case in dB)	30			dB

no	spec	condition	min	typ	max	unit
Complex Baseband filter						
3.1	Supply current	I+Q			2	mA
3.2	Filter order	Butterworth		3		
3.3	complex filter center frequency	BDR and EDR modes		0.9 1.8		MHz
3.4	complex Filter 3dB bandwidth	BDR and EDR modes		1.4 2.8		MHz
3.3	average input referred noise	over 1MHz/2MHz BW for BDR/EDR modes	35	30	20	nV/sqrt(Hz)
3.4	Voltage gain	Passband	17	18	19	dB
3.5	AGC range			5		dB
3.6	AGC gain step		0.8	1	1.2	dB
3.7	IIP3	Inband 2-tones with in-band IM3	-9	-6		dBVrms
3.8	OP1dB	At filter output	1.2			Vpp
3.9	Rejection (BDR)	2MHz offset from center	20			dB
		3MHz offset from center	30			
		6MHz offset from center	50			
3.10	Passband ripple/droop	over 1MHz/2MHz BW for BDR/EDR modes			±0.5	dB
3.11	Passband group-delay ripple	pk-pk over desired signal BW			190	ns
3.12	Filter tuning accuracy	Variation of filter 3dB over PVT			±5	%
3.13	output DC offset	montecarlo over 30+ samples			±50	mV
3.14	input/output common-mode DC voltage	to interface with mixer and ADC	550	600	650	mV
3.15	Image rejection	montecarlo over 30+ samples	25			dB
3.16	Filter loading	Differential, resistor // capacitor		15kΩ 1pF		

no	spec	condition	min	typ	max	unit
VCO and LOgen						
4.1	Supply current	VCO core, includes dynamic current			3	mA
		/2 divider for 50% I/Q LO			1	
		VCO buffer to drive /2			0.5	
4.2	VCO Frequency range		4.8		5.0	GHz
4.3	VCO Phase noise (5GHz, SSB)	100kHz offset		-90		dBc/Hz
		1MHz offset		-115		
		3MHz offset		-125		
		10MHz offset		-135		
4.4	KVCO (5GHz)	Over cap-bank and over 0.3V-0.9V Vtune range	30	60	100	MHz/V
4.5	Supply pushing	20% step on supply			500	kHz/V
4.6	Load pulling	Load at VCO buffer out (/2) on/off			200	kHz pp
4.7	/2 I/Q quad. phase accuracy	4.5-sigma			3°	degrees

Some biasing hint:



If you need a constant-gm biasing, you can build one or use a macromodel for it.

GOOD LUCK!