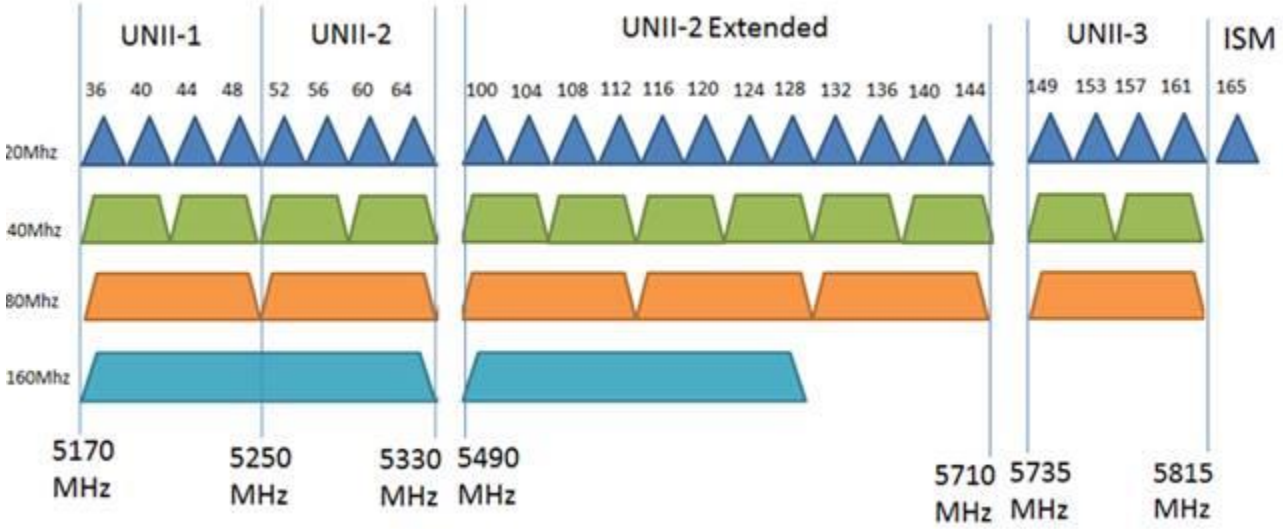
VCO design

- **VCO design**
  - Elements comprising a VCO (overview)
  - Tank design
  - Minimizing VCO phase noise
  - VCO bias
  - VCO supply pushing
  - VCO load pulling

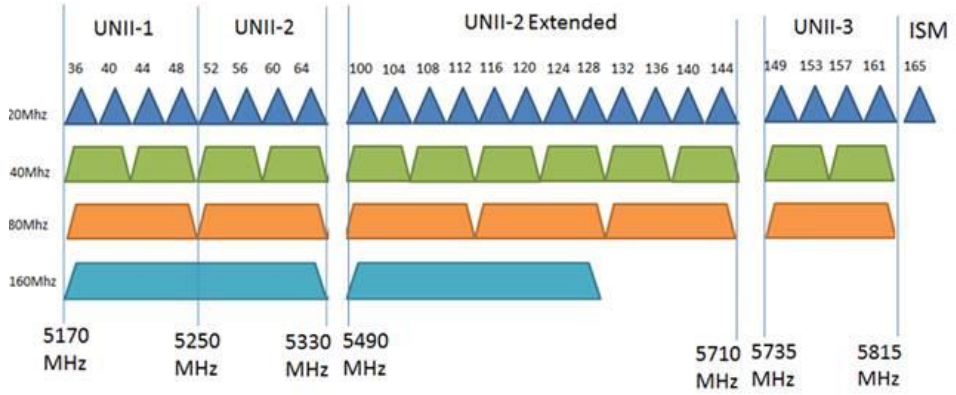
  - **references**

Why a VCO is needed?:



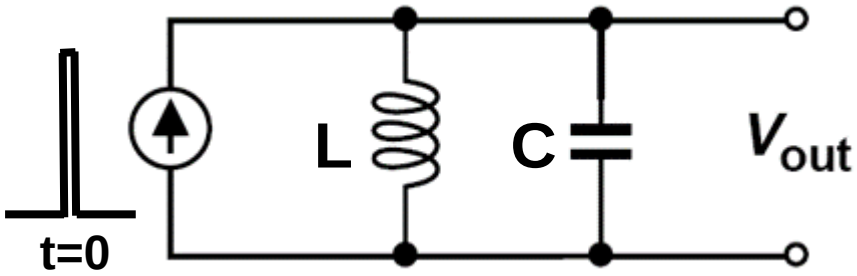
- The above example shows the WiFi channels for A-band. In order to select the correct channel, an LO source with “controllable” precise variable frequency is needed to drive the mixer at the right channel for down-conversion (Rx) or up-conversion (Tx)
- such variable-controlled LO scheme is composed of a Synthesizer (PLL) and an LO-generation scheme (LOgen)
- The Voltage Controlled Oscillator, VCO, is a key element to build a synthesizer

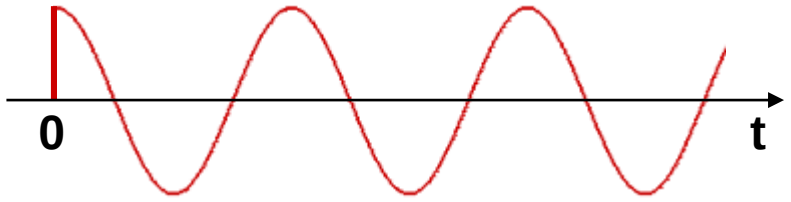
Elements comprising a VCO:

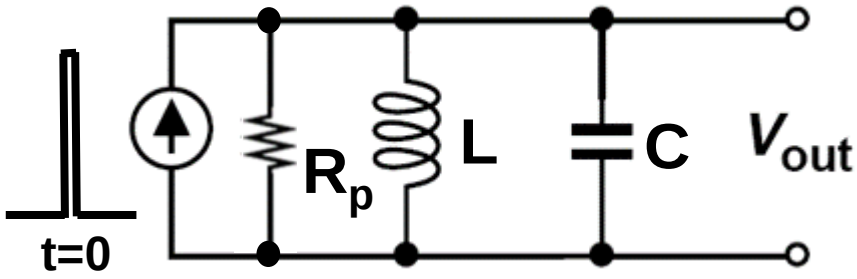


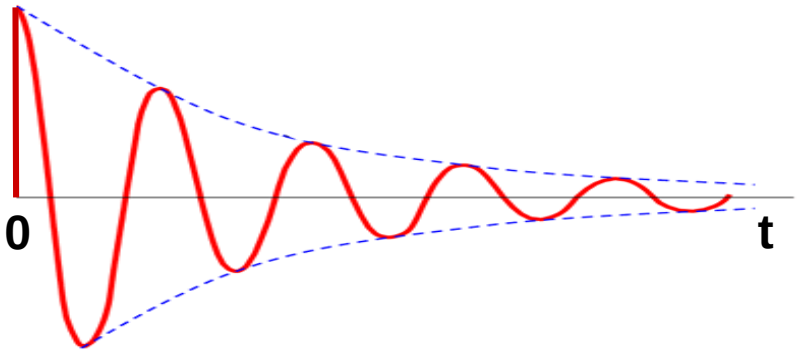
- A VCO would then has a resonance circuit whose center frequency is shifted by some sort of a controlling voltage (sometimes current). This is usually done by a variable capacitor (or called Varactor)
- As seen from the above example, the VCO needs to be able to be tuned over a given (sometimes wide) tuning range. In the above example, the LO needs to cover ~650MHz range. Such wide range cannot practically be covered only by a varactor, so a switchable capacitor bank is needed to divide the wide band into smaller sub-bands (coarse frequency shift to the VCO tank).
- Because of the loss of the tank, an active circuit is needed to keep injecting energy into the lossy tank to sustain oscillation

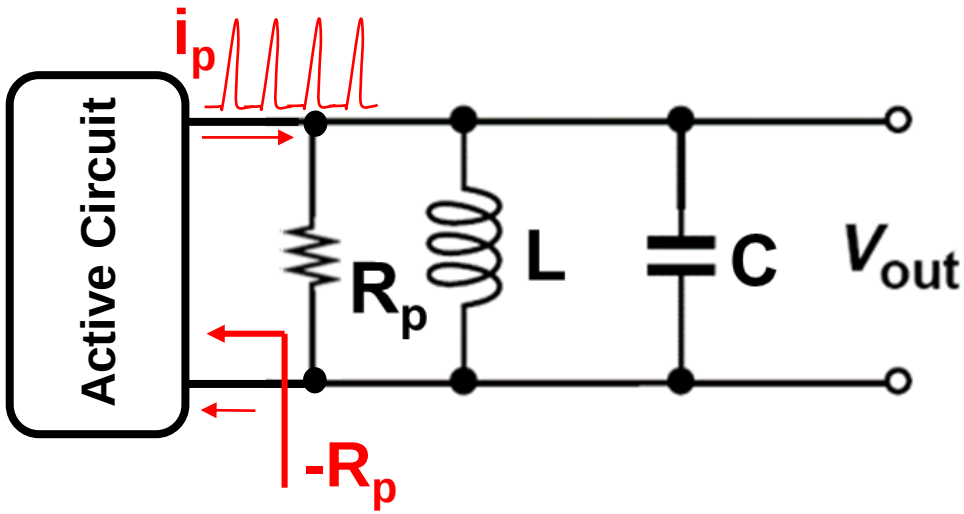
Purpose of an active circuit in VCO:

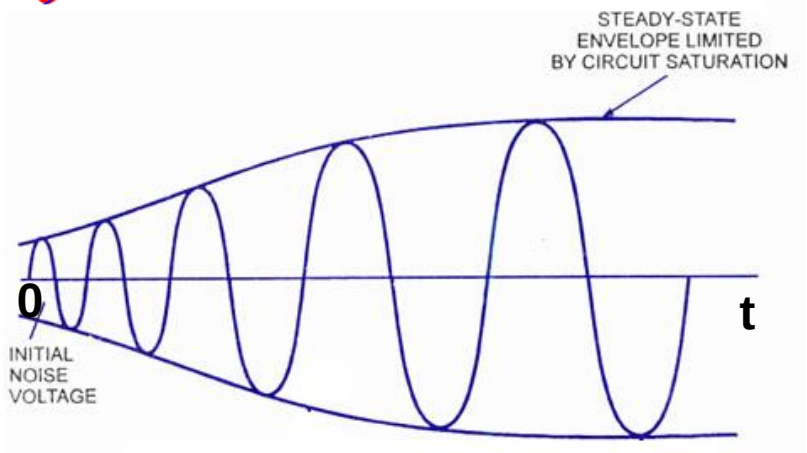




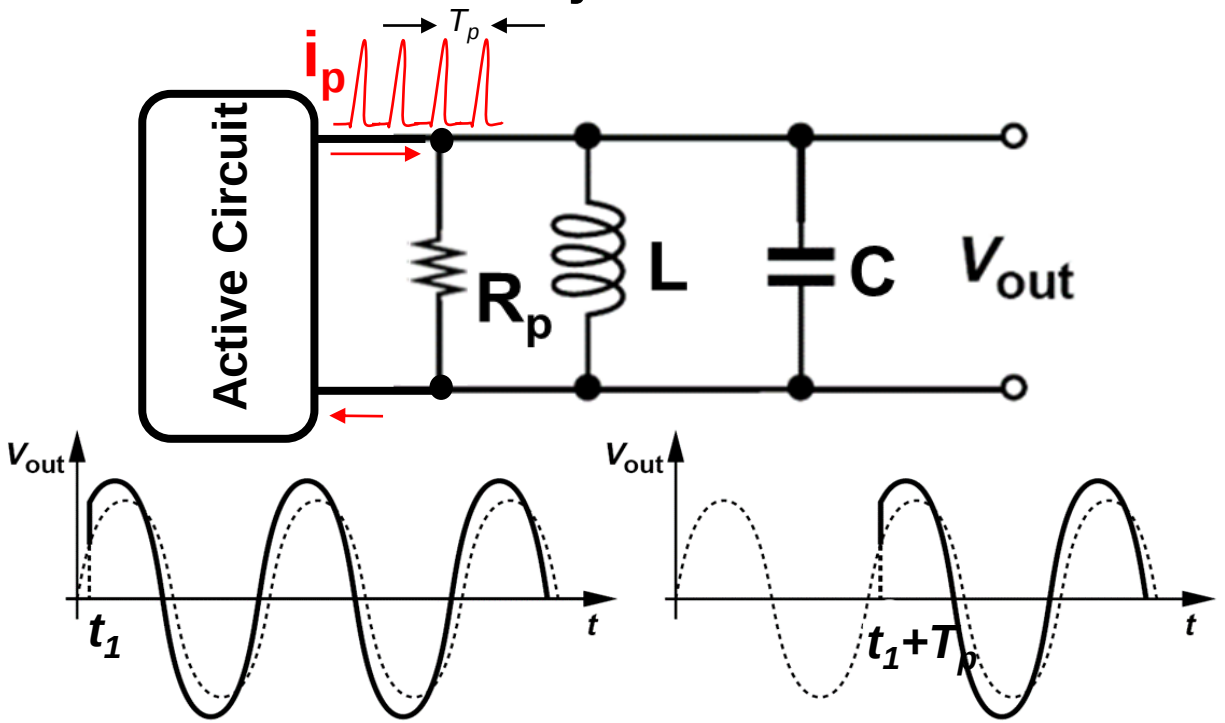






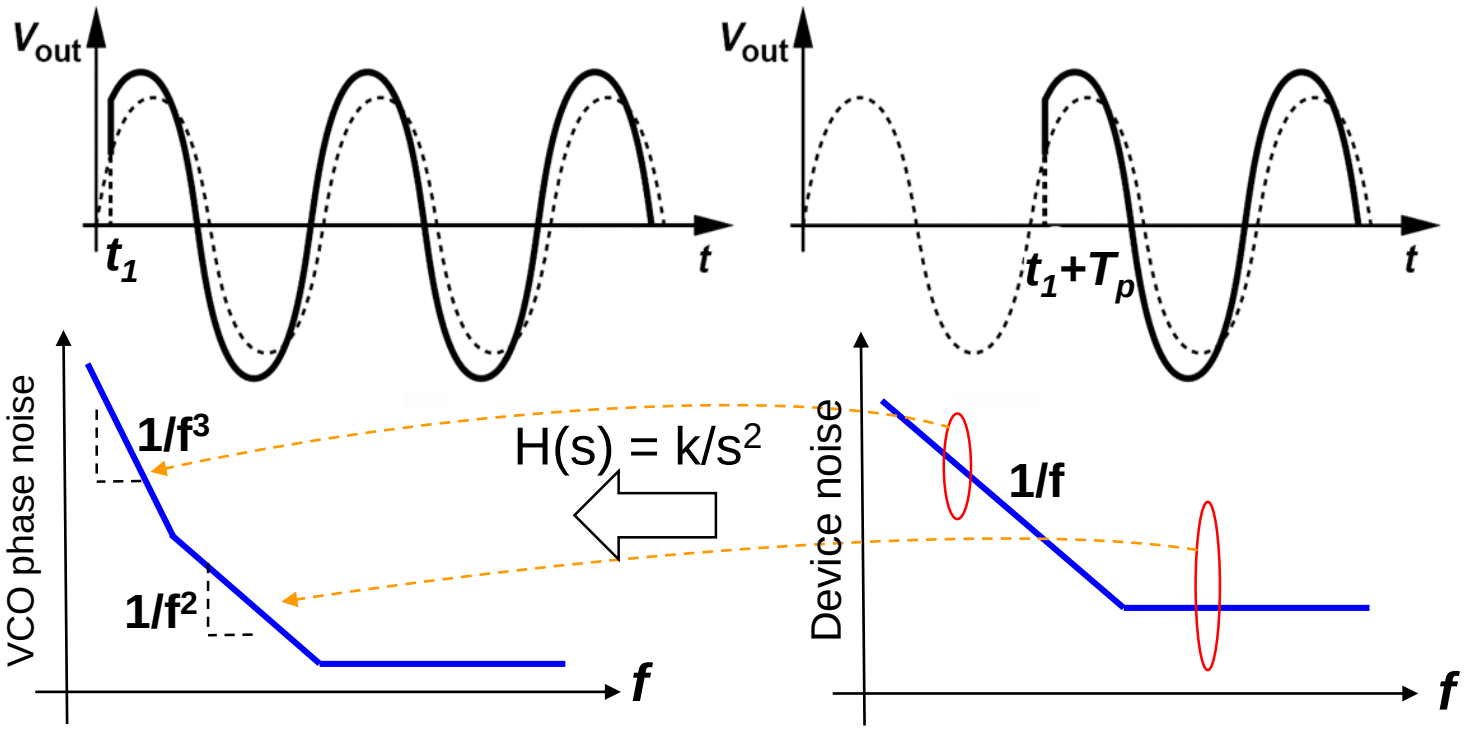


VCO Active circuit noise injection:



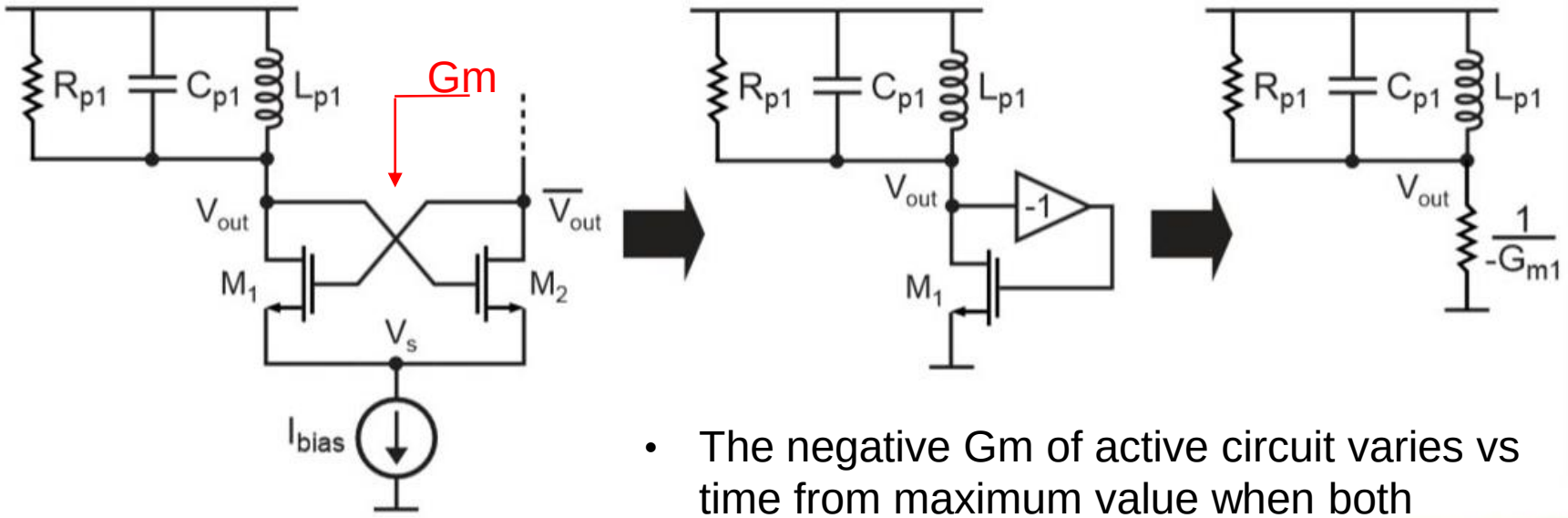
- each cycle, the active circuit injects noise along with its AC current
- Injected noise results in altering the phase of VCO output (indefinitely). Since injected noise is random, the associated phase alteration of VCO output is also random (phase noise).
- Different VCO topologies (Colpitts, Pierce, Hartley, etc) differ in reducing impact of injected noise on phase noise. Injecting noise at zero crossing gives worst phase noise while injecting it at peaks gives least impact on phase noise

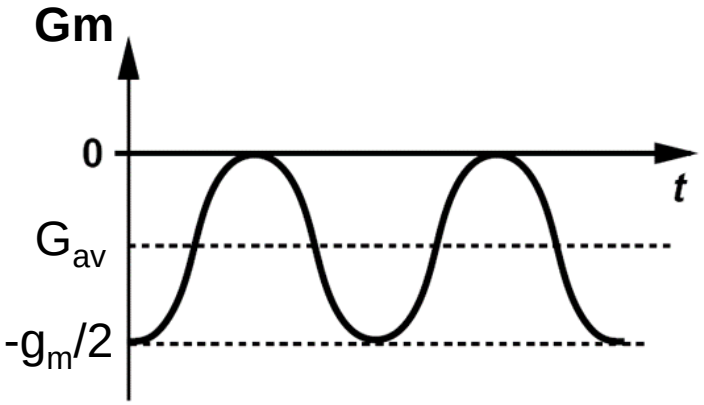
VCO Active circuit noise injection:



- Because each cycle active circuit adds random noise resulting in changing phase of VCO indefinitely, phase noise then in a sense has an integrator (accumulator) transfer function of device noise.
- As a result, device noise transforms into phase noise by an $H(s) = k/s^2$. This means the "flat" or white noise of the device transforms into a "$1/f^2$ region of phase noise while device flicker noise results in a "$1/f^3$ region of phase noise

Negative gm of active circuit:

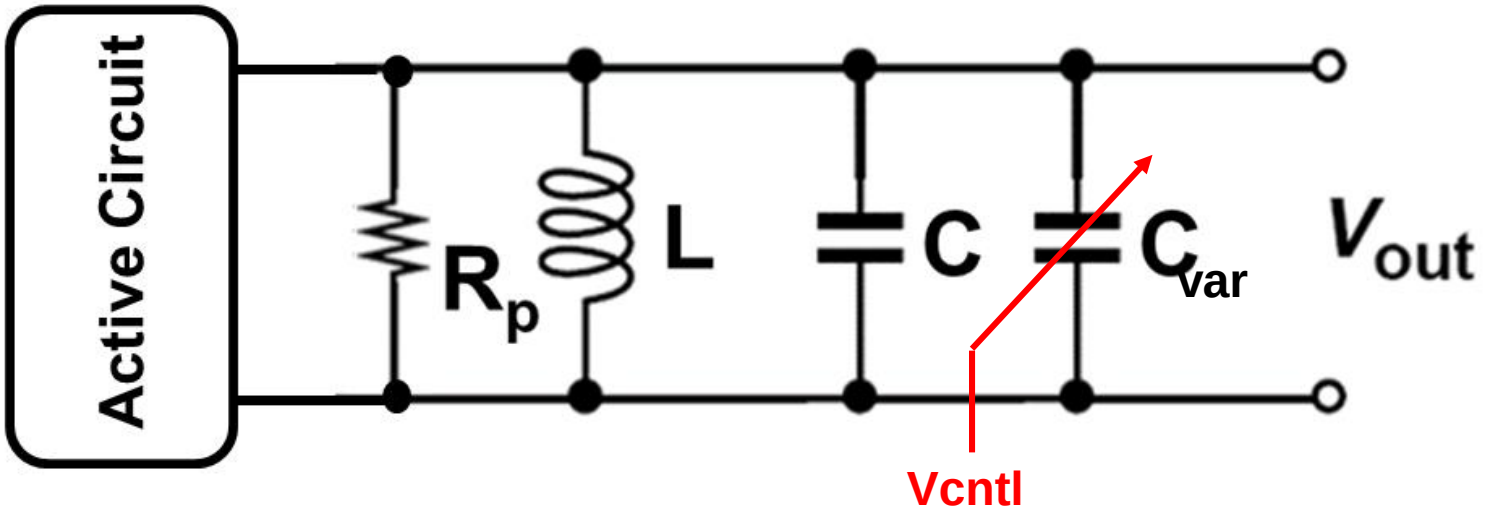




- The negative Gm of active circuit varies vs time from maximum value when both transistors are on and conduct same current to minimum of 0 when one transistor shuts off.

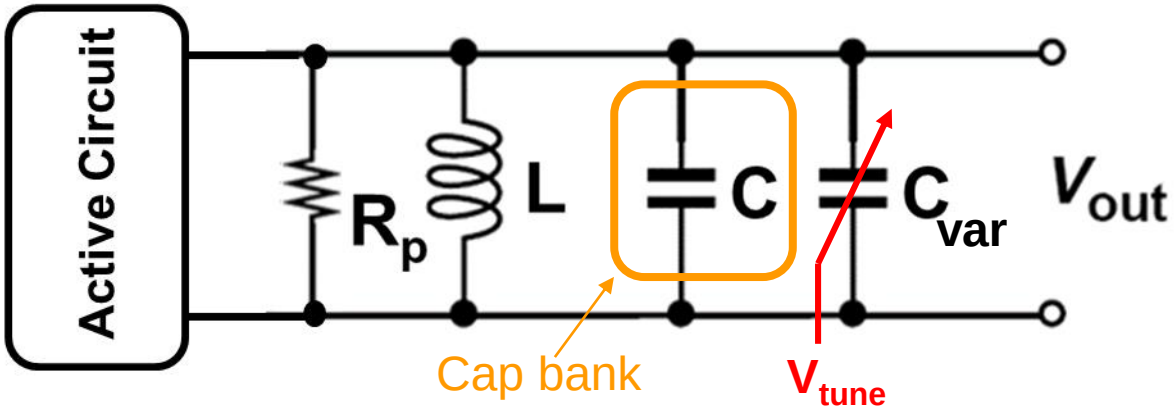
When negative Gm is at max (| Gm |>$1/R_p$), oscillation grows until one transistor shuts of and negative gm drops to 0, in this case oscillation starts to decay. Obviously the average steady-stage negative Gm (G_{av}) should equal the loss of the tank $1/R_p$

One more tank element: Variable-capacitor (varactor):



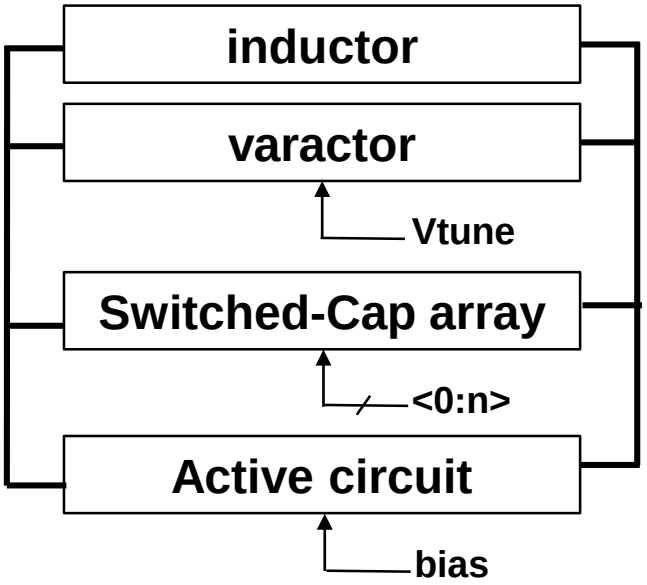
- As discussed earlier, a VCO need to be able to shift/change its frequency in response to some control voltage. As a result a varactor, whose capacitance changes with voltage is an ideal element for that
- The varactor size determines how much output frequency changes as a function of the control voltage (KVCO)
- However, varactors also converts the noise at its terminals (from control voltage and from tank) into phase noise. Therefore KVCO cannot be made too large.

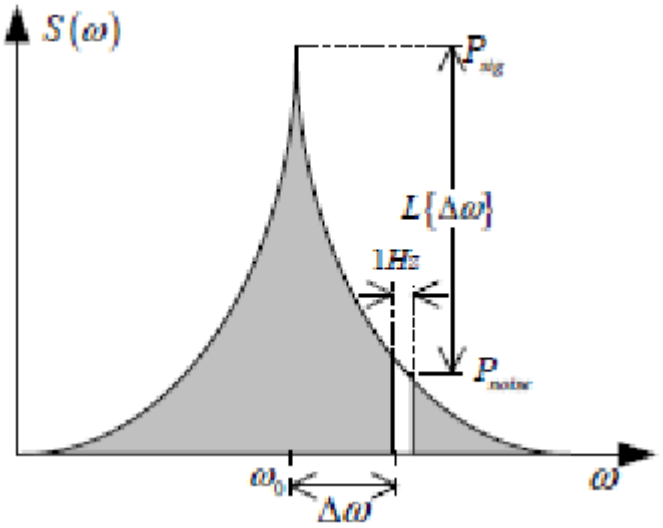
Why we need both MoM cap and varactor in VCO tank:



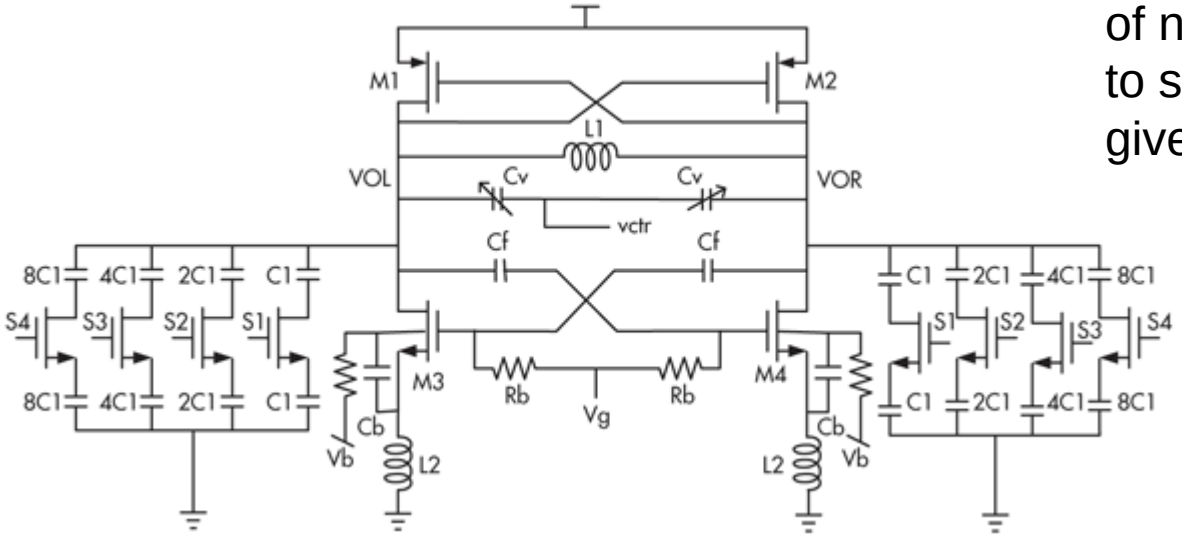
- V_{tune} voltage range is quite limited. It usually comes from a PLL whose output is set by its charge-pump compliance range (V_{dsat} to V_{dd}-V_{dsat}). For V_{DD} of 1.2V, this range is limited to say 0.6V.
- A WiFi 11a has 650MHz RF band. If we use a VCO with 2x RF frequency (to accommodate for the I/Q LO DIV2), the VCO minimum tuning range is 1.3GHz. If we want to add margin to this to cover process and temperature variation of +/-20% we end up with 1.82GHz. If this entire range is to be covered by a single varactor, KVCO needs to be 1.82GHz/0.6V or ~3GHz/V. This is a very high value and can result in bad phase noise due such large varactor converting noise into phase noise.
- As a result, the frequency range in divided into smaller sub-bands, each is covered by one shared small varactor and a set of switchable MoM capacitor bank.

How a typical VCO looks like:





- Phase noise in is the ratio of noise power in 1Hz BW to signal power (10log(ratio) gives dBc/Hz)

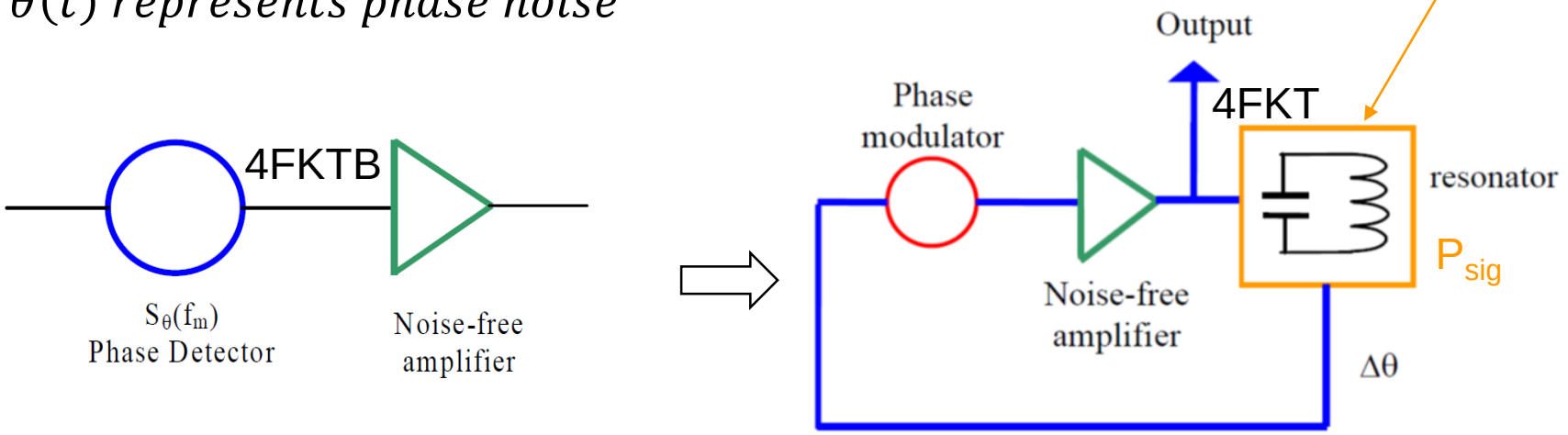


VCO phase noise: The Leeson's formula

$$VCO_{out} = A\cos(\omega_0 t + \theta(t))$$

$\theta(t)$ *represents phase noise*

$$\theta_{out}(f_m) = \left(1 + \frac{f_0}{j2Q_L f_m}\right)\theta_{in}$$

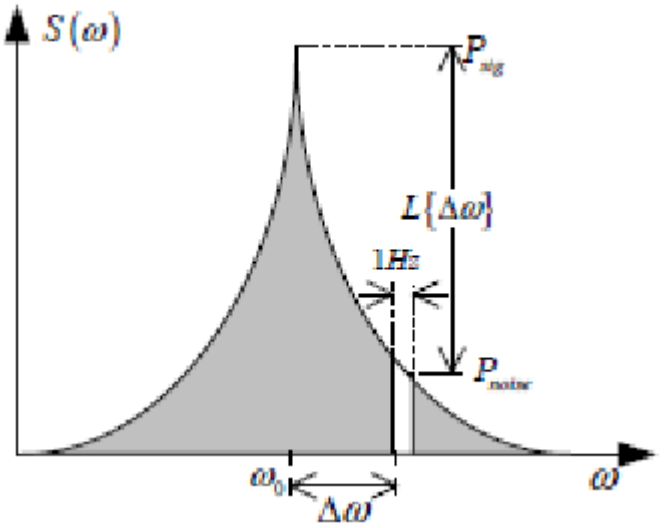


- A VCO can be modeled as a unity positive feedback amplifier with phase detector at it input. The amplifier has a noise density at the input equal to its unmatched noise factor (F) times 4KTB
- The condition of oscillation is when gain around the loop is "1" and phase is 360-degrees.
- This means at oscillation, the noise density at the output is also 4FKTB. Since phase noise compares the signal power to phase noise in 1Hz BW → B=1

VCO phase noise: The Leeson's formula

$$L(\Delta\omega) = 10\log\left[\frac{2FkT}{P_{sig}}\cdot\left(1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right)\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right]$$

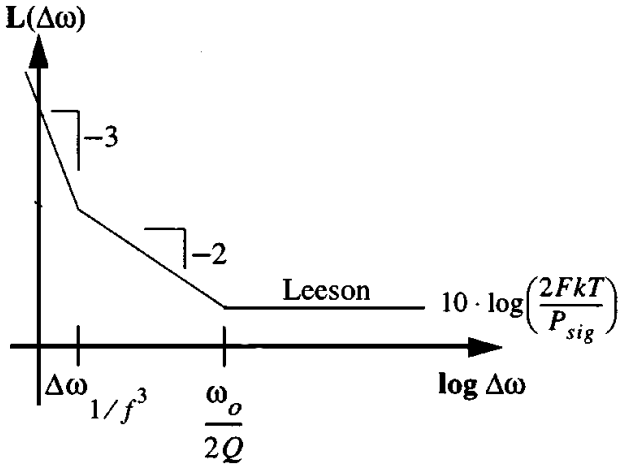
1/f² 1/f³



- VCO design optimization tries to achieve target phase noise over the required tuning range at lowest possible power consumption (and die area). People call this best FoM.

- Phase noise improves with larger tank swing (higher P_{sig}) and higher tank Q with lowest device noise

- therefore, VCO design is all about:
  - tank design and Q optimization
  - VCO device sizing and biasing for lowest noise
  - achieve highest VCO swing limited by device reliability, Vdd and power consumption limits



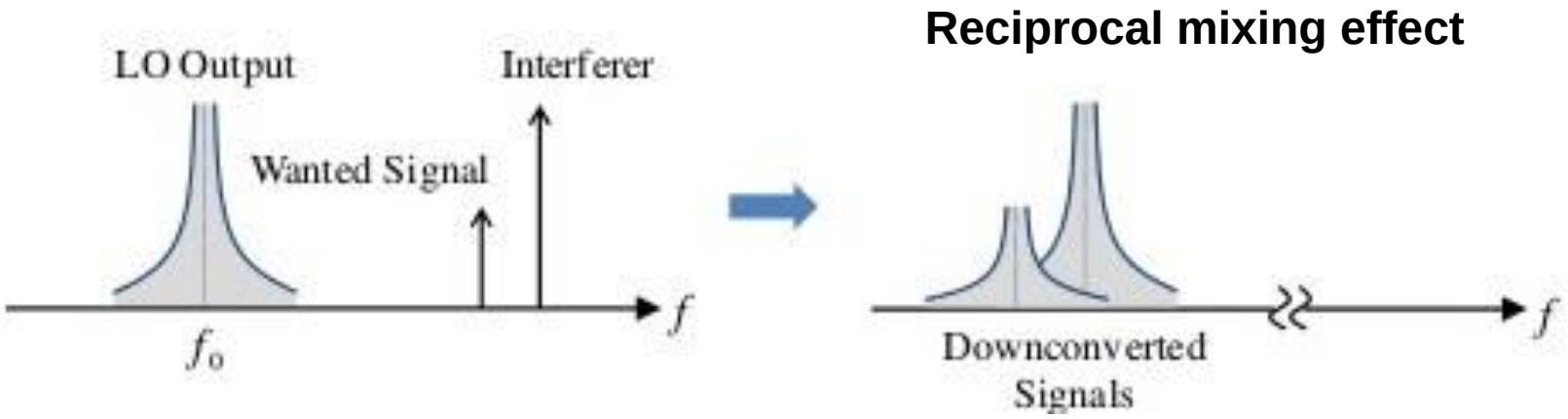
Phase noise theory:

- There are many theories pertaining to VCO phase noise. The most prominent of those are:
  - The linear time invariant based theory. Most are a derivative of the Leeson formula. Such formulas give a *limited* insight on important VCO elements to take care of for best phase noise
  - The linear time variant based theory. This theory gives good estimation of impact of noise sources to VCO phase noise for a *given design* but still does not give enough design guideline on how to optimize the VCO for a given topology.
- The reader is advised to read the EE242 lecture on phase noise theory by prof. Niknejad:

http://rfic.eecs.berkeley.edu/ee242/pdf/Module_7_2_PhaseNoise.pdf

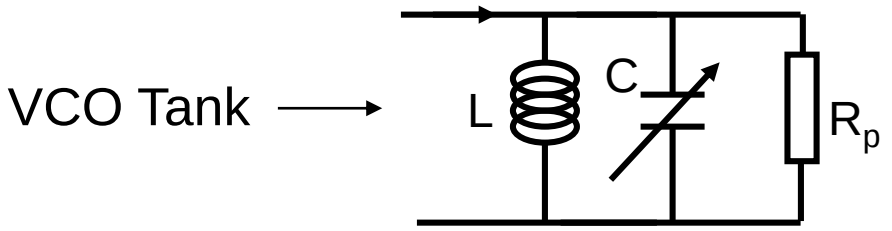
- In this lecture, we will try to add some insight on how to design and optimize different sections of an LC VCO

Why phase noise is important



- As we discussed in previous lectures, phase noise impacts received signal in two different ways:
  - in-band SNR (hence in-band EVM) via integrated phase error of LO (double-side integration of phase noise)
  - In-band SNR in presence of nearby large blocker via reciprocal mixing (single-side integration of blocker phase noise over signal BW)
- Similarly, in transmitters, transmitted signal SNR (in-band EVM) is impacted by LO IPE. Also out of band emission (ACLR) is set by out of band phase noise.

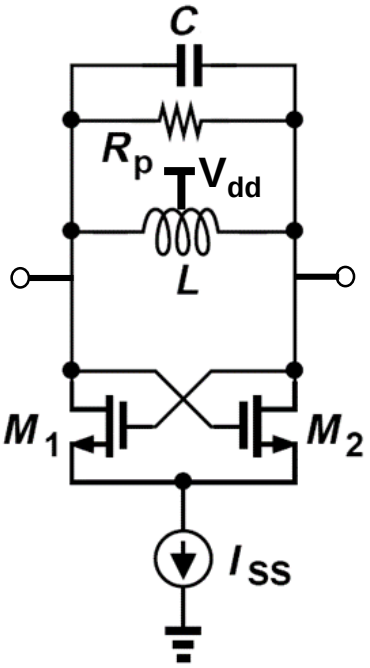
VCO tank design:



$$R_p \approx \omega LQ$$

- VCO design is 60% tank design!
- Per the Leeson formula, phase noise improves with larger tank swing. Swing = I_{vco} * R_p , where R_p is the equivalent tank shunt loss, and I_{vco} is VCO current
- How to maximize swing without burning too much power?
  - How to chose L and C values?
  - inductor Q vs. area tradeoff, what are the boundaries?

Current-limited and V_{dd}-limited regimes of VCO:



- initially VCO swing (peak) is set by (I_{SS} * R_p). Phase noise improves by 6dB each time you double I_{SS} (ignoring noise from active devices, in reality improvement is 4~5dB). In this case, the VCO is considered operating in the "current-limited regime".
- However, the VCO swing cannot increase indefinitely. Its upper limit is set by V_{dd}. Once VCO swing saturates , its phase noise no longer improves with increasing I_{SS} (it improves only slightly due to sharper rise/fall time of signal which improves noise). In this case, VCO is considered operating in the "voltage limited regime"

Choice of inductor:

- there is an infinite L x C combination that resonates at the desired frequency. Which combination is best?
- The phase noise equation of an LC VCO is given by the simplified Leeson's formula:

$$PN(f_m) \approx 10\log\left[\frac{4kTR_{noise}}{V_{osc}^2}\frac{1}{4Q_L^2}\left(\frac{f_0}{f_m}\right)^2\right]$$

Where R_{noise} is the equivalent noise resistance across the tank, V_{osc} is the peak oscillation swing, Q_L is the loaded tank quality factor, f_0 is the oscillation freq., f_m is the offset freq.

Let us assume the tank Q is dominated by that of an inductor. This is a true assumption as long as the varactor and capacitor Q are large. For example, let us assume the element Q is 15, 30 and 60 for inductor, varactor and mom cap, respectively. Also let us assume the varactor capacitance is 0.1x of the total tank cap. At resonance, the total loaded tank Q can be calculated as:

$$Q_L^{-1} = Q_{ind}^{-1} + 0.1Q_{\text{var}}^{-1} + 0.9Q_C^{-1} = \frac{1}{15} + \frac{0.1}{30} + \frac{0.9}{60}$$

$$\Rightarrow Q_L \approx 11.8$$

Obviously there is an error in our assumption, and it grows as the inductor Q gets higher or the varactor/MoM-cap Q gets smaller.

Therefore for now, we assume $R_p \approx \omega_0 Q_{ind} L$, where R_p is the tank loss. Moreover, $V_{osc}=I_{bias}R_p$. Therefore, the phase noise equation can be rewritten to be:

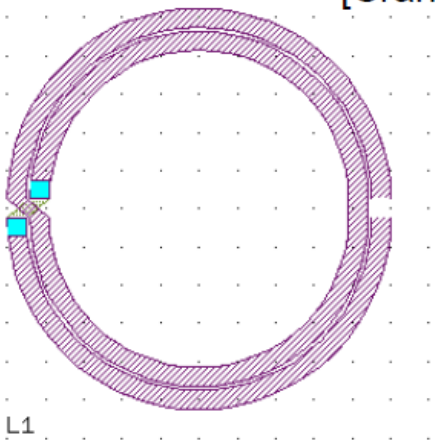
$$PN(f_m) = \frac{4kTR_{noise}}{I_{bias}^2 \omega_0^2 Q_{ind}^2 L^2} \frac{1}{4Q_{ind}^2} \left(\frac{f_0}{f_m}\right)^2 = \frac{4kTR_{noise}}{I_{bias}^2 f_m^2} \left(\frac{1}{4\pi L Q_{ind}^2}\right)^2$$

It can be seen that to minimize phase noise, the term LQ^2_{ind} must be maximized. In other words, look for the inductor with maximum LQ^2.

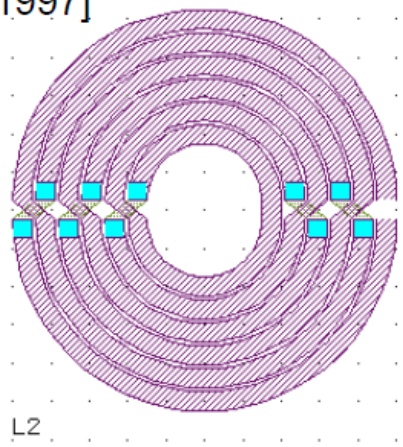
Limitations:

Maximizing LQ^2 means going for a large outer diameter for an inductor of a given inductance. The limit, of course, is the maximum area which can be tolerated. The other option is to use the largest inductor possible. This however means smaller capacitance required for resonance. The upper limit of inductor value is set when the parasitic capacitance becomes a big portion of the overall capacitance required for resonance, or when the variable capacitance becomes much smaller to cover the tune range as will be seen later.

[Craninckx, JSSC, May 1997]



Inductor with high Q

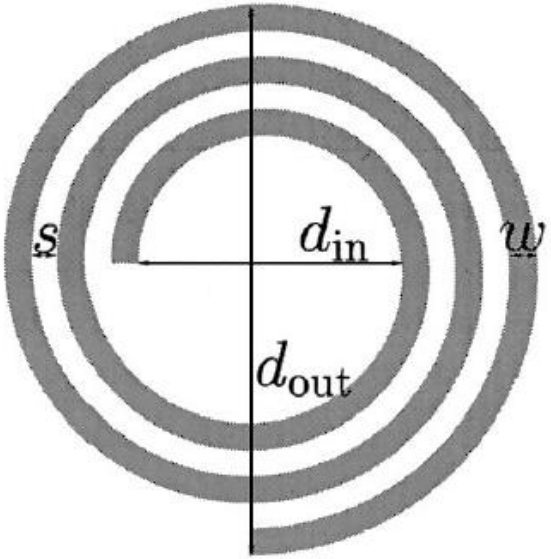


Inductor with low Q

$Q = \frac{\omega L}{R_S}$; where Rs is the series resistance of the inductor wires (ignoring loss to substrate)

- Inner turns contribute little to self inductance but they contribute a lot to series resistance → degrade Q
- As a result, hollow inductor offers higher Q
- However, when we also considering loss to substrate, less turns means larger inductor area which leads to larger substrate loss.
- As a result, an optimum number of turns exists when we consider both series loss and shunt loss

Single turn vs multi-turn inductance:



Wheeler formula

$$L = \mu_0 \cdot K_1 \cdot \frac{N^2 d_{avg}}{1 + K_2 \rho}; \left(\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}}, d_{avg} = \frac{d_{out} + d_{in}}{2}\right)$$

K_1, K_2 are geometry dependent coefficients (value depend on shape: square, hexagonal, octagonal, etc.)

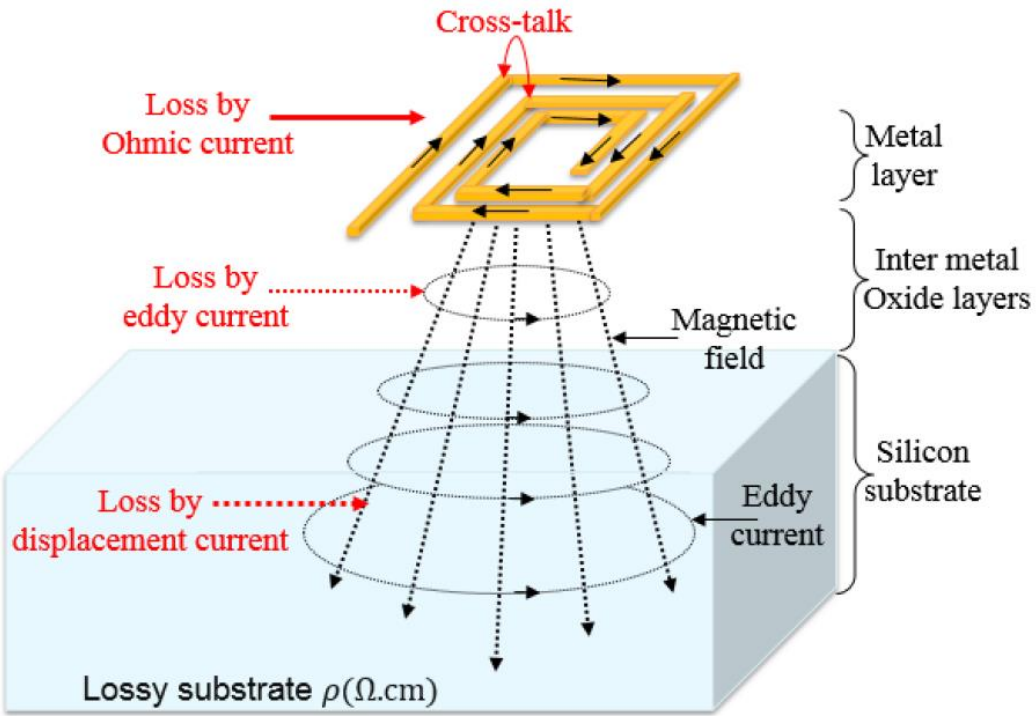
$$R_{dc} = R_{sh} \pi \cdot N^2 / \rho$$

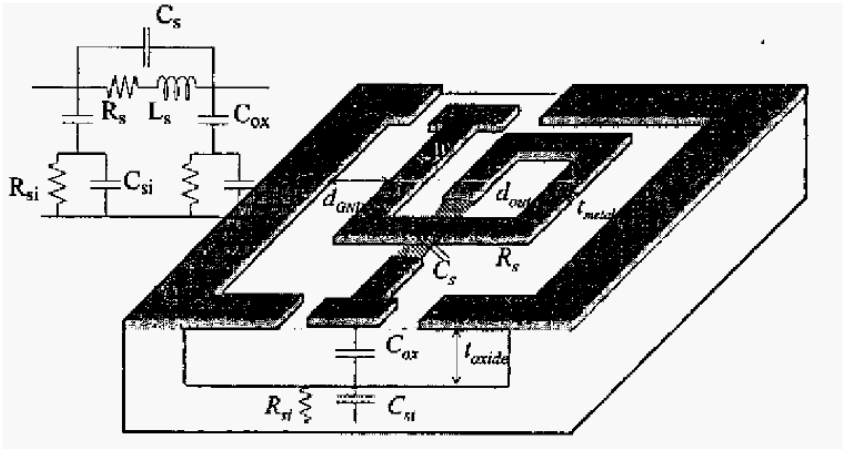
If a single-turn and a 2-turn inductors ought to have same Q (assume is set by R_{dc}) and same inductance (we will define ρ_1, d_{avg1} and ρ_2, d_{avg2} are for single and two turn inductors, respectively):

$$\Rightarrow \rho_2 = 4\rho_1, \qquad d_{avg_1} = 4 d_{avg\,2} \frac{1 + K_2 \rho_2 / 4}{1 + K_2 \rho_2}$$

- This result in the single-turn inductor area to be much larger than that of a 2-turn inductor (~5 times)!

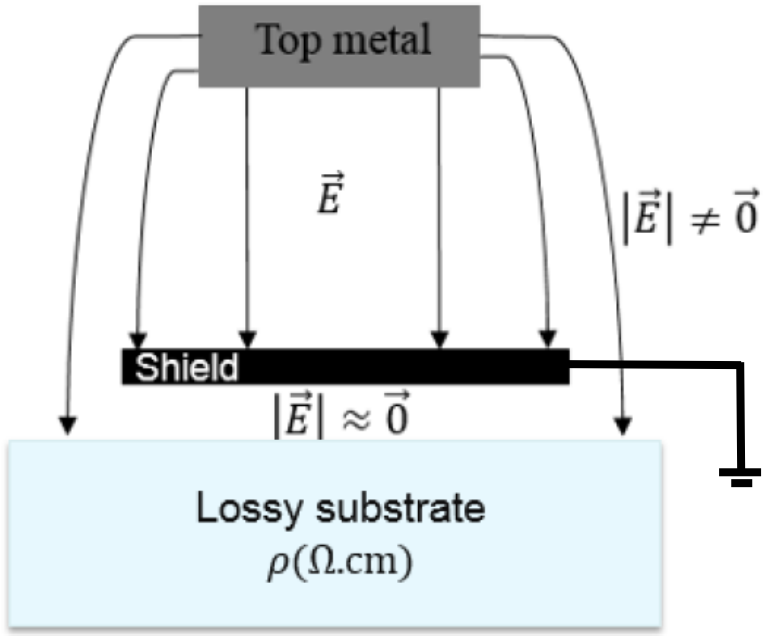
Impact on substrate loss:





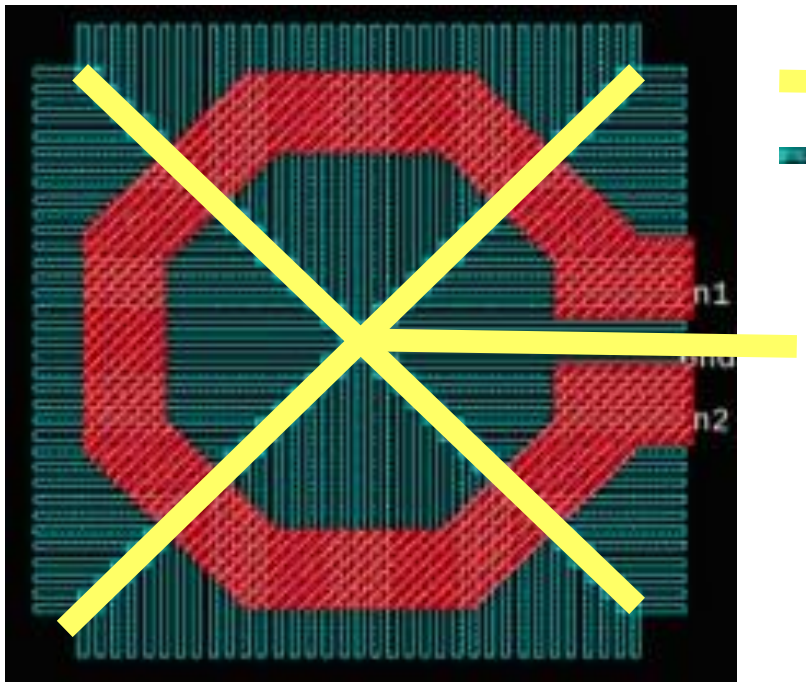
- The inductor body is coupled to the lossy substrate via oxide capacitance
- Two loss mechanisms happen in the substrate:
  - Electric: Substrate loss de-Q the inductor via the parasitic coupling cap
  - Magnetic: via Eddy current loss into the substrate

Pattern Ground Shield (PGS):



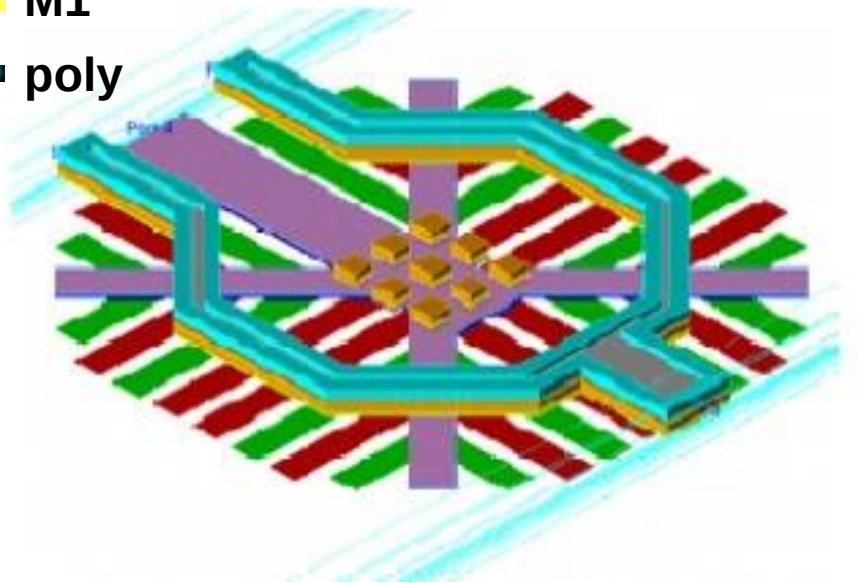
- A conductive shield beneath the inductor (when shield connected to ground) helps terminate electric fields and prevent them from going to the lossy substrate → improve Q
- However, the shield does nothing to magnetic field → how to prevent Eddy current in the shield itself?
- Use a finger-like pattern shield perpendicular to the inductor wiring

Pattern Ground Shield (PGS):



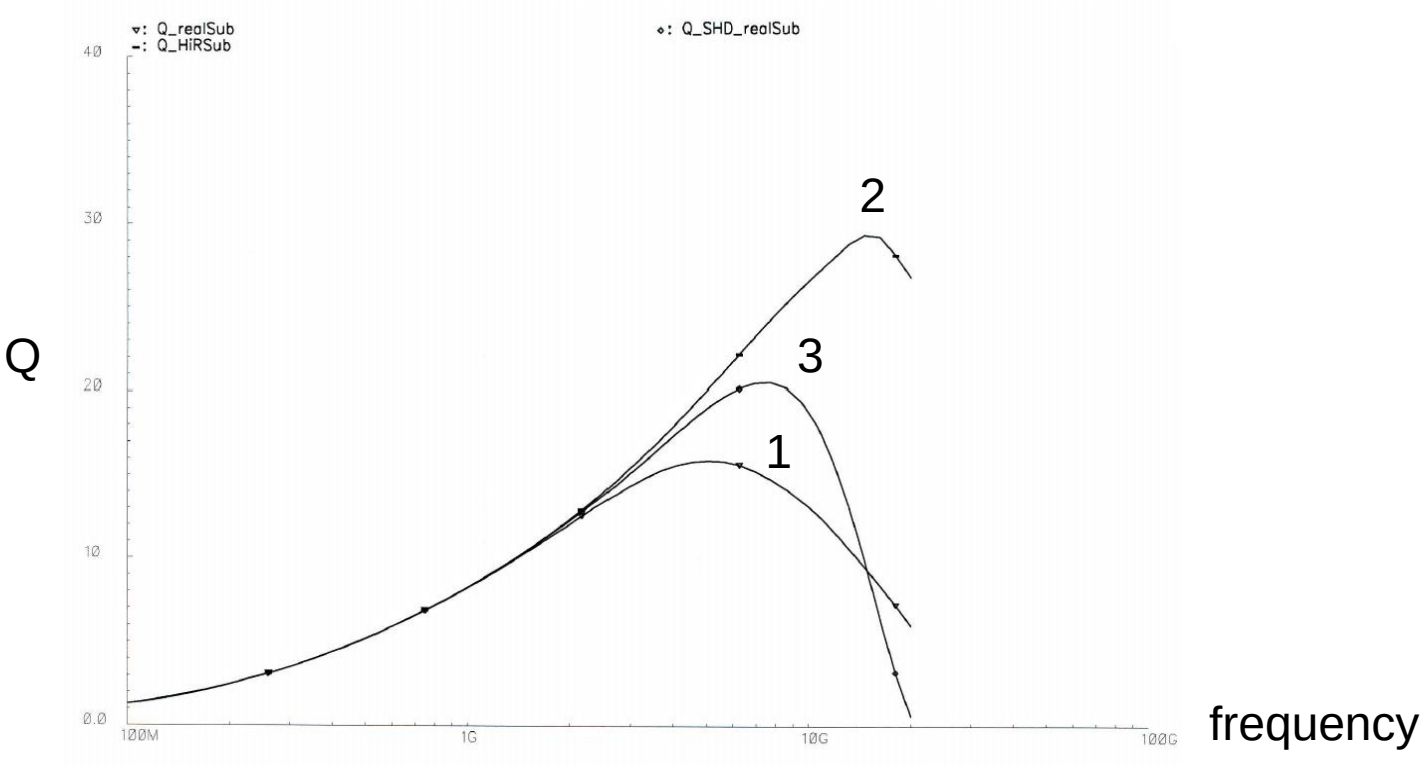
M1

poly



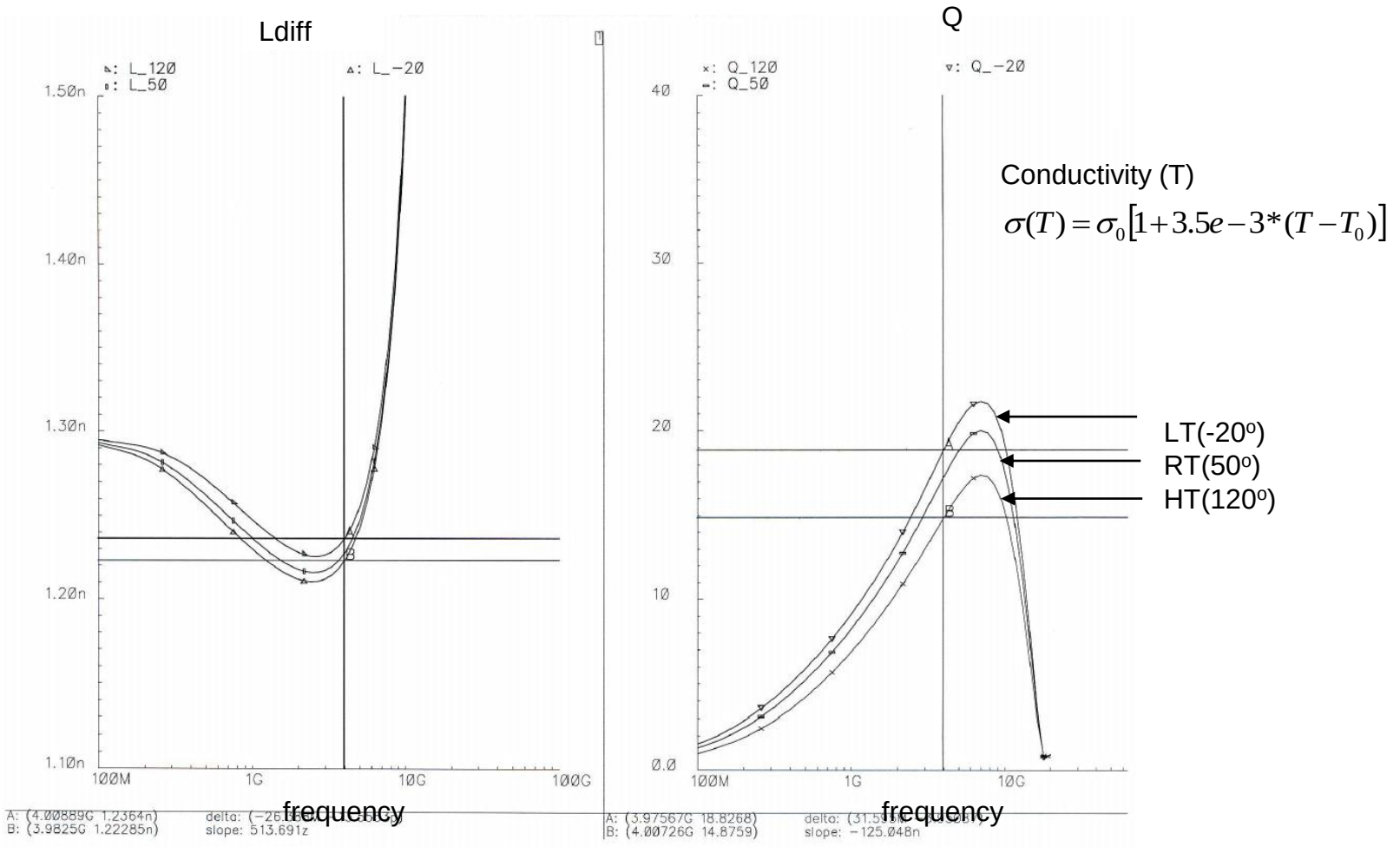
- PGS provides a well defined ground reference for VCO tank return current.
- Shield with slots perpendicular to inductor routing to prevent eddy current loss in the shield.
- Use silicide poly to construct PGS for low resistance and also lowest cap to inductor body (boosts inductor self-resonance frequency)
- Shielding should be extend from shield to inductor (>=2X inductor wire width) to terminate fringing fields

Pattern Ground Shield (PGS):



- 1. Real substrate → substrate loss + Eddy current loss
- 2. High resistivity substrate → No substrate loss (only metal loss)
- 3. real substrate with inductor ground shielding → some Eddy current loss + shield loss

A typical inductor Inductance and Q plots vs frequency

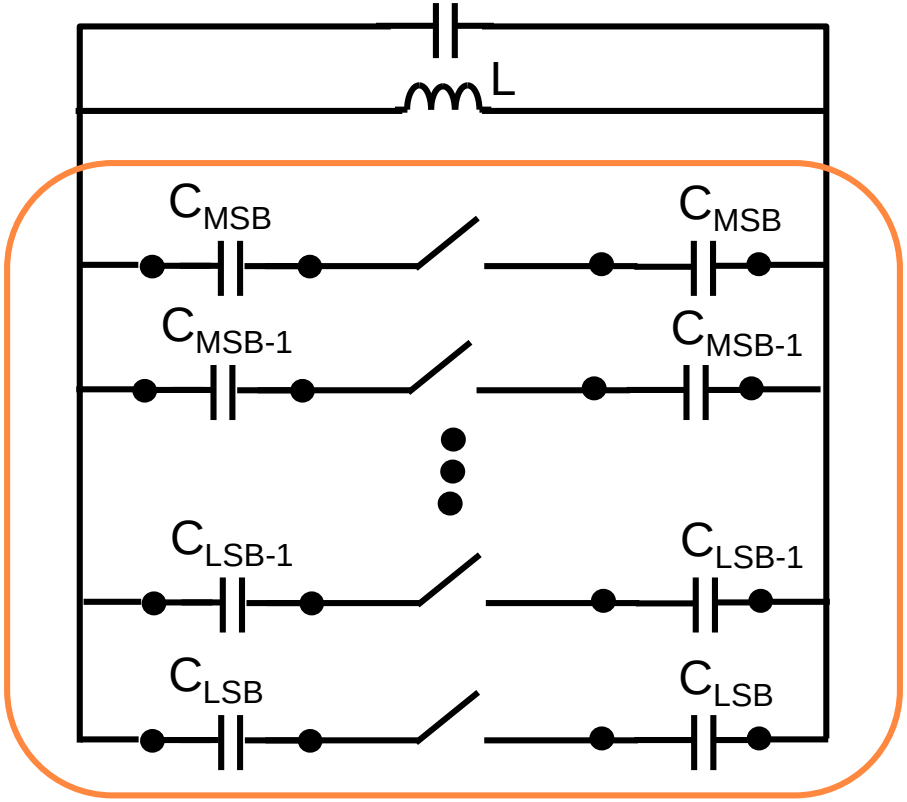


- Better to design inductor so operating frequency is slightly below the peak-Q

Designing capacitor bank

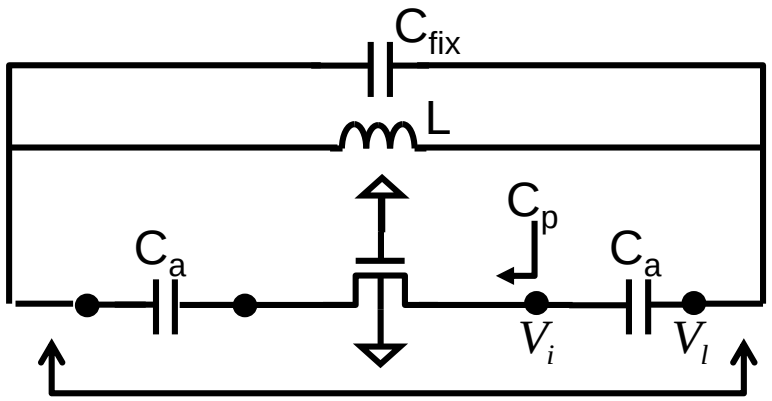
$C_{fix} = C_{active} + C_{buffer} + C_{wiring}$

Tuning range: $f_{min} \sim f_{max}$
$C_{max}/C_{min} = (f_{max}/ f_{min})^2$



- When all cap bank switches are ON, the VCO should oscillate at f_{min}. When all switches are off, the only capacitance left at the tank is $C_{fix} + C_{off}$ of the OFF cap-bank with VCO oscillating at f_{max}.
- Usually f_{min} and f_{max} are wider than guaranteed VCO tuning range to accommodate for process and temperature variation

Designing capacitor bank: procedure



$$C_{on} = 0.5 \cdot C_a, \qquad C_{off} = 0.5 \cdot \frac{C_a \cdot C_p}{C_a + C_p}$$

1. 1st order calculation for f_{max} and f_{min}:

Tuning range: $f_{min} \sim f_{max}$
Target $f_{min} = f_{min}/1.05$
Target $f_{max} = 1.05 \times f_{max}$
(5% extended range from each end to account for process variation and temp)

$C_{max}/C_{min} = (f_{max}/ f_{min})^2$

$C_{fix} = C_{active} + C_{buffer} + C_{wiring}$

2. Find C_{on}, C_{off}, and C_{fix} values

Tuning range: $f_{min} \sim f_{max}$
Given tank inductance L
→ $C_{min} = 1/L(2\pi f_{max})^2$
→ $C_{max} = 1/L(2\pi f_{min})^2$

$C_{min} = C_{fix} + C_{off}$
$C_{max} = C_{fix} + C_{on}$
→ Calculate C_{on} , C_{off}

Designing capacitor bank: Example

Operating freq range:
3.980E+09
4.775E+09

VCO coverage range:
ΔC 0.2 (+/-20%) **Based on process corner model file** $\frac{1}{\sqrt{1.2\times1.02}}=0.9$, $\frac{1}{\sqrt{0.8\times0.98}}=1.13$
ΔL 0.02 (+/- 2%)
Fmin 3.524E+09 (> min Subband @ typical) $3.98GHz \div 1.13$
Fmax 5.283E+09 (< max Subband @ typical) $4.775GHz \div 0.9$

$$KVCO = frequency \times \left(\sqrt{\frac{C_{tot}}{C_{tot} + dC_v / dV}} - 1 \right)$$

frequency	L	Ctot	Ccbank	Cfix	dCv/dV (F/V)	KVCO(MHz/V)
5.283E+09	3.390E-09	2.677E-13	1.677E-13	1.000E-13	-1.020E-14	100.63
4.775E+09	3.304E-09	3.362E-13	2.362E-13	1.000E-13	-1.020E-14	72.43
3.980E+09	3.174E-09	5.038E-13	4.038E-13	1.000E-13	-1.020E-14	40.29
3.524E+09	3.126E-09	6.525E-13	5.525E-13	1.000E-13	-1.020E-14	27.54

Within Required KVCO

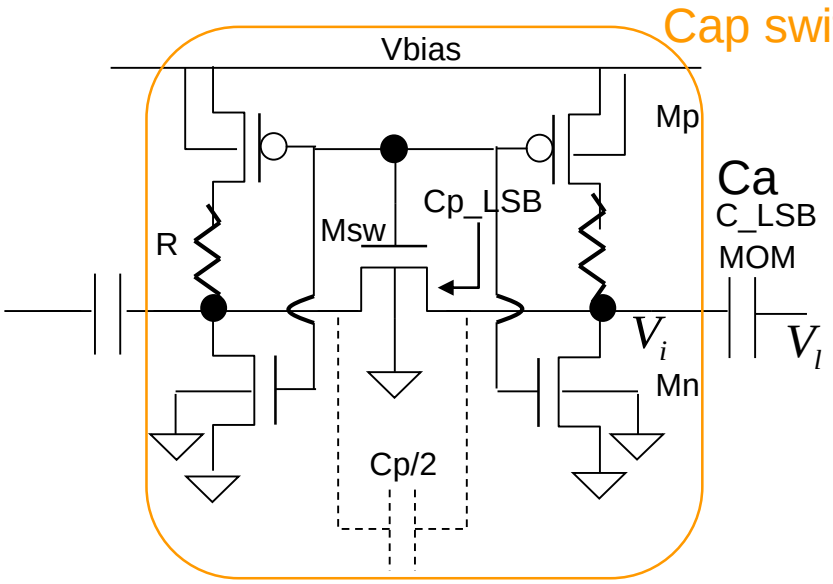
Ccbank Cmax-Cmin = 3.85E-13

$C_{\max} \equiv C_{on}, \quad C_{\min} \equiv C_{off}$

Δ varac C
required curves $= \frac{C_{\max} - C_{\min}}{\Delta C_{\text{var}ac}}$

1.53E-15 → **Based on Vtune range: 0.3V ~ 0.9V**
251.466245 → **8-bit cap array**

Designing capacitor bank: design and size cap switch



4. Find the switch device size for LSB

Let us assume an 8-bit cap-bank

$C_{\_LSB} = 2.\ C_{on}/255$

$C_{P\_LSB} = 2.\ C_{off}/255$

→ $C_{\_MSB} = C_{\_LSB} \times 128$

$C_{P\_MSB} = C_{P\_LSB} \times 128$

size switch so target Cp value to meet both reliability as well as Q of cap is met

3. Find the C_{off}/C_{on} ratio

V_l max = *A* Vpp, which can be found from sim

V_i max = *a* Vpp, limited by NCS stress of switch device (OFF)

→ $C_p/C_{on} = (A/a) - 1$

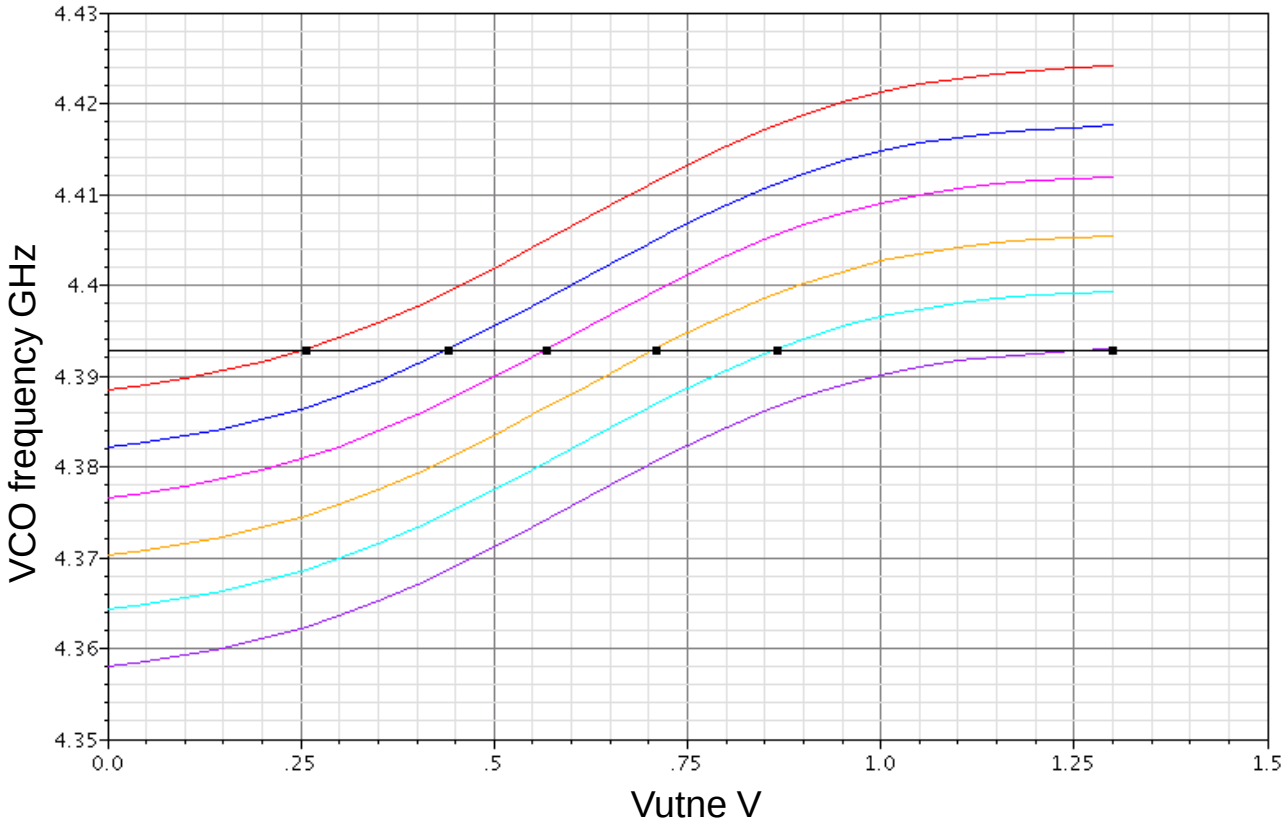
→ $C_{off}/C_{on} = 1 - a/A$

$$C_{off} = \frac{C_a C_p}{C_a + C_p} \quad ; \quad \frac{V_i}{V_l} = \frac{a}{A} = \frac{C_a}{C_a + C_p}$$

5. Size R to provide sufficient Q.

- Size Mp PMOS switch Ron to let the Vds swing <10m~50mV to reduce AM-PM
- Chose Vbias large enough so nmos switch Msw drain/source diffusion diode does not turn on but not too large to cause reliability stress to that device
- Size Mn as small as possible (their job is just to set DC voltage at MoM cap node when Msw is on

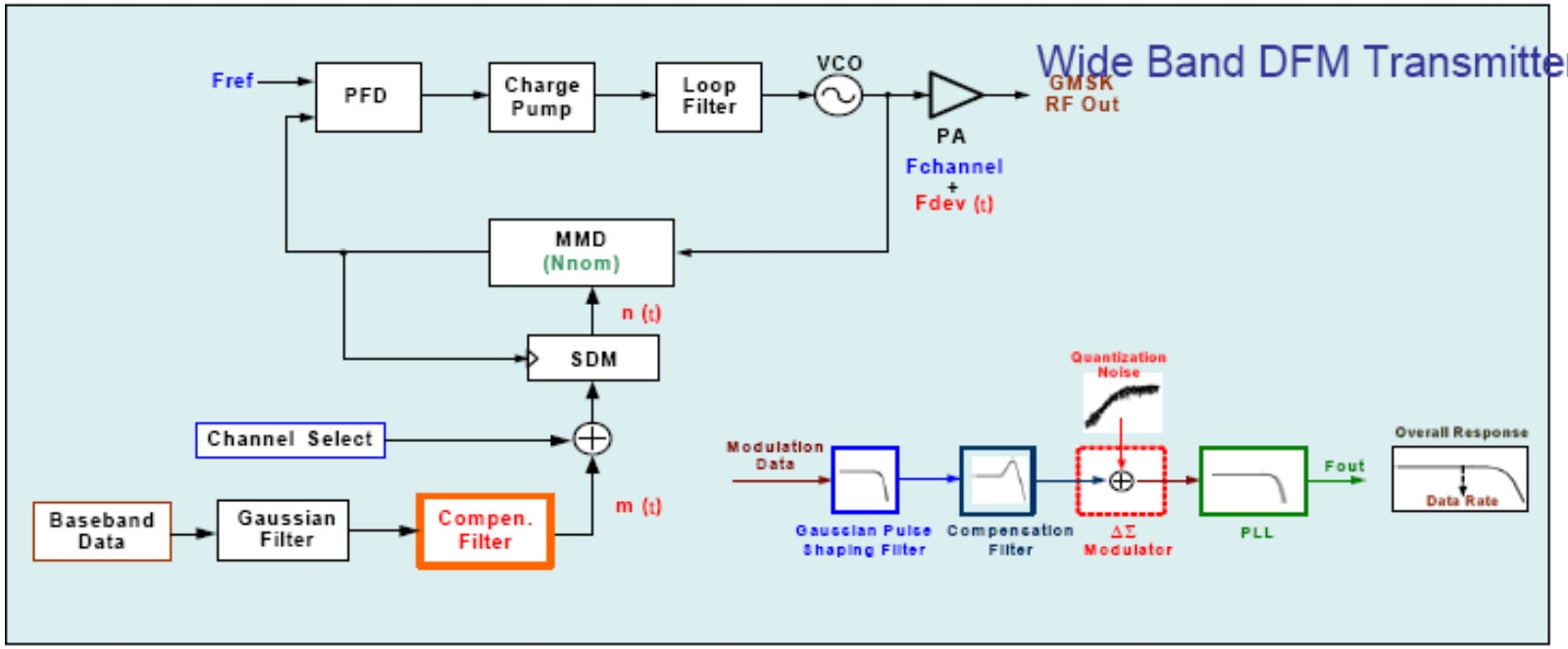
How many cap bank bits I need? cap bank overlap



6 cap banks from the 255 cap bank example

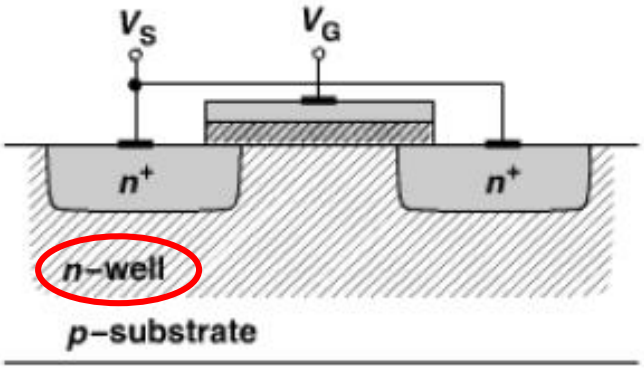
- For any frequency point within the VCO coverage range, there must exist multiple cap banks that can cover that particular frequency point. Not satisfying this requirement could result in “gaps” in the cap bank over PVT with frequencies that cannot be covered. Usually having min of 3 cap banks to cover any given frequency is enough

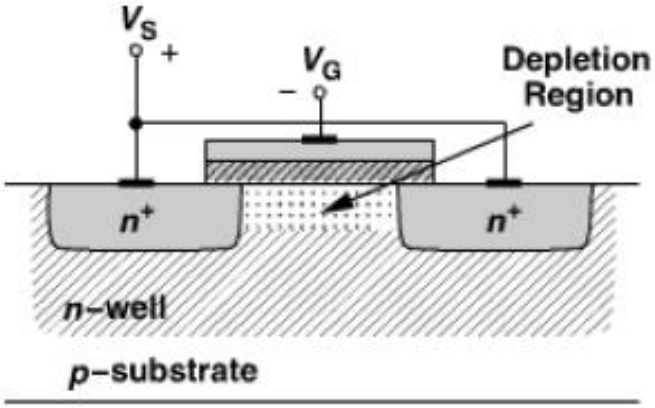
Varactor design: why a linear varactor

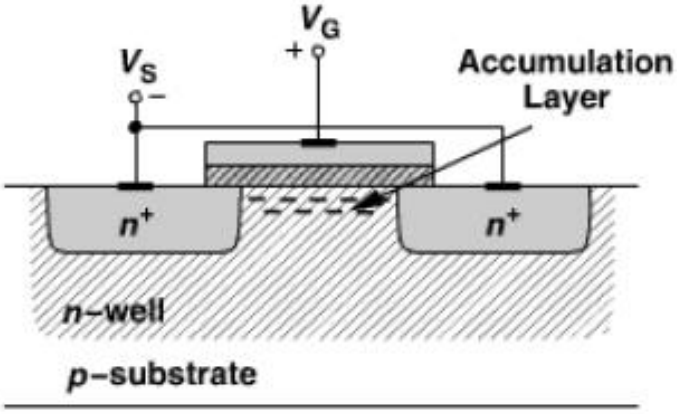


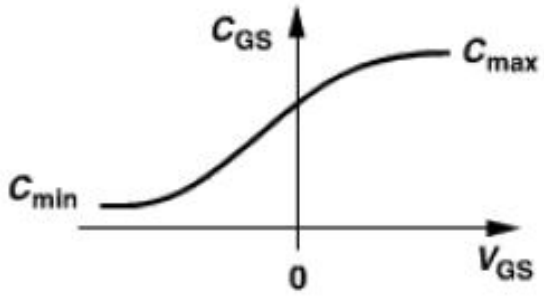
- In normal synthesizer, a Nonlinear VCO V-f characteristic causes strong AM-PM conversion of amplitude noise due to VCO circuits. It also causes loop bandwidth to change a lot over tune voltage causing large loop bandwidth variation and so phase noise (requires margin in PLL design and/or adaptive loop filter design)
- In direct frequency modulation (DFM) transmitter, the information is applied to the input of sigma-delta modulated synthesizer which enforces VCO to follow the information. Nonlinear VCO V-f characteristic causes loop bandwidth to change during modulation, potentially degrade modulation accuracy due to limited loop bandwidth

Varactor design: accumulation-mode nwell nmos varactor

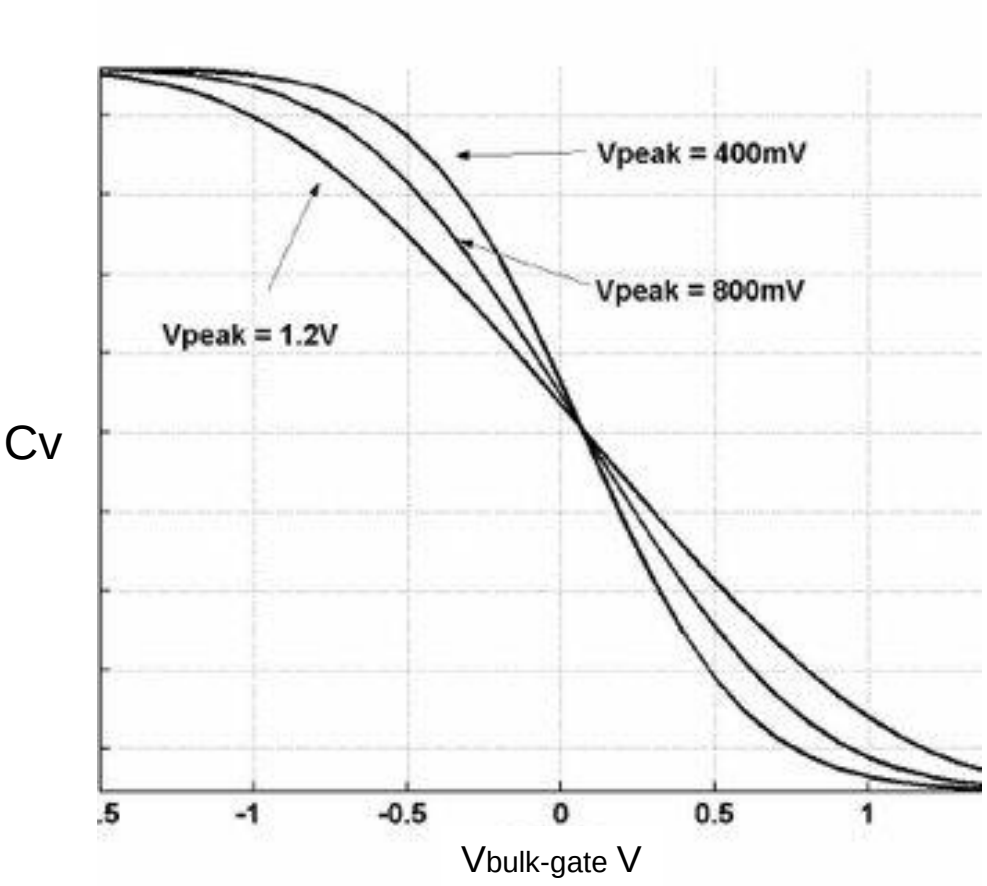


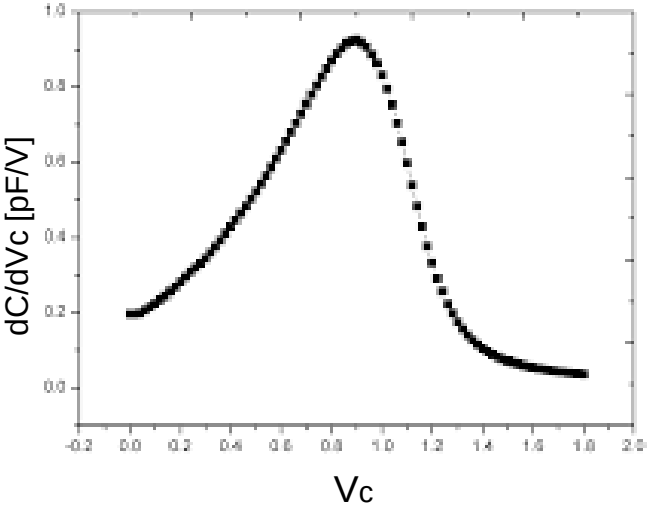






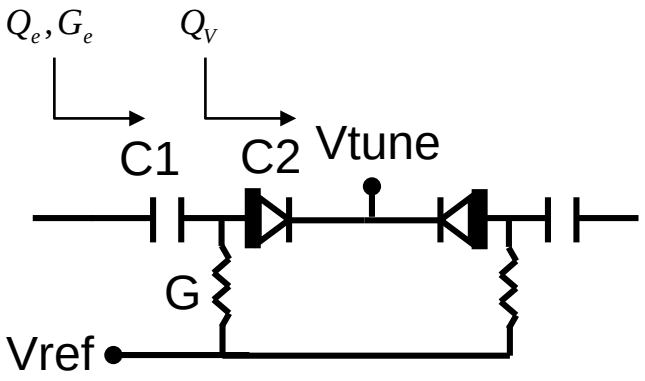
Varactor design: accumulation-mode nwell nmos varactor





- The nmos varactor gets more “linear” as swing across it gets larger. Its Kv also changes. This is important to note when designing PLL to realize the exact Kv of this varactor for better loop design and so loop dynamics

Varactor design: some design consideration



$$G_e = G \cdot \left(\frac{C_1}{C_1 + C_2}\right)^2$$ ← Important for loss

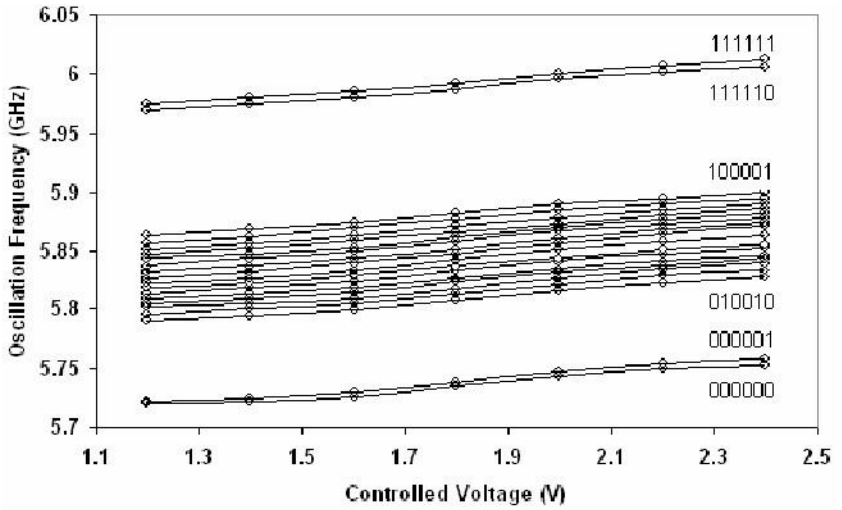
$$C_e = \frac{C_1 \cdot C_2}{C_1 + C_2}$$

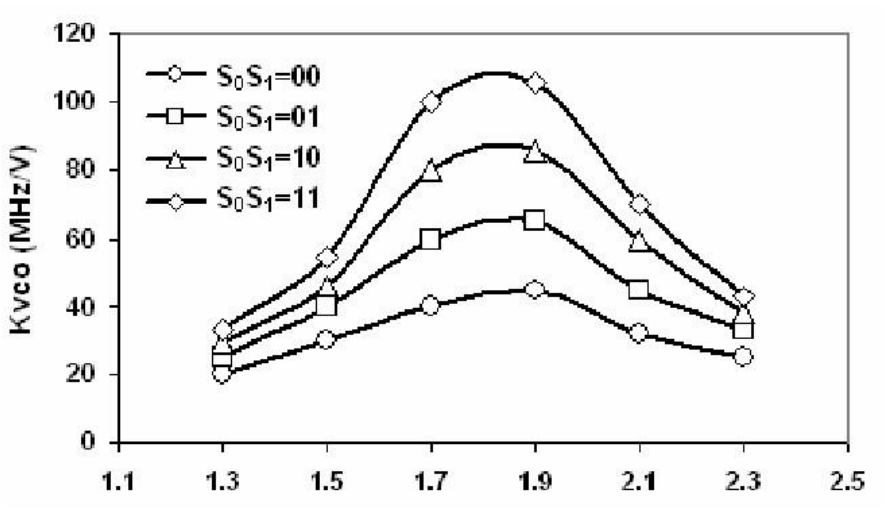
$$\Rightarrow Q_e = \frac{\omega \cdot C_e}{G_e} = \frac{\omega \cdot C_2}{G} \cdot \left(\frac{C_1 + C_2}{C_1}\right) = Q_v \cdot \left(1 + \frac{C_2}{C_1}\right)$$

- *G* and *Vref* are to provide bias to the varactor. Vref is usually chosen in mid-range of Vtune. C1 is an AC coupling cap to isolate varactor bias from tank DC voltage.
- Varactor size is set by target Kvco (set by PLL and also phase noise)

- Determine G so as not to load the tank but also not contribute noise → sweep G and find optimum value for phase noise
- Determine C1 and C2 (varctor W x L x Finger size for best Qv), maximize the swing across varactor (increase C1) but prevent G_e from loading the tank.
- Choose Vref at the middle of the “flat” region of the Kv curve

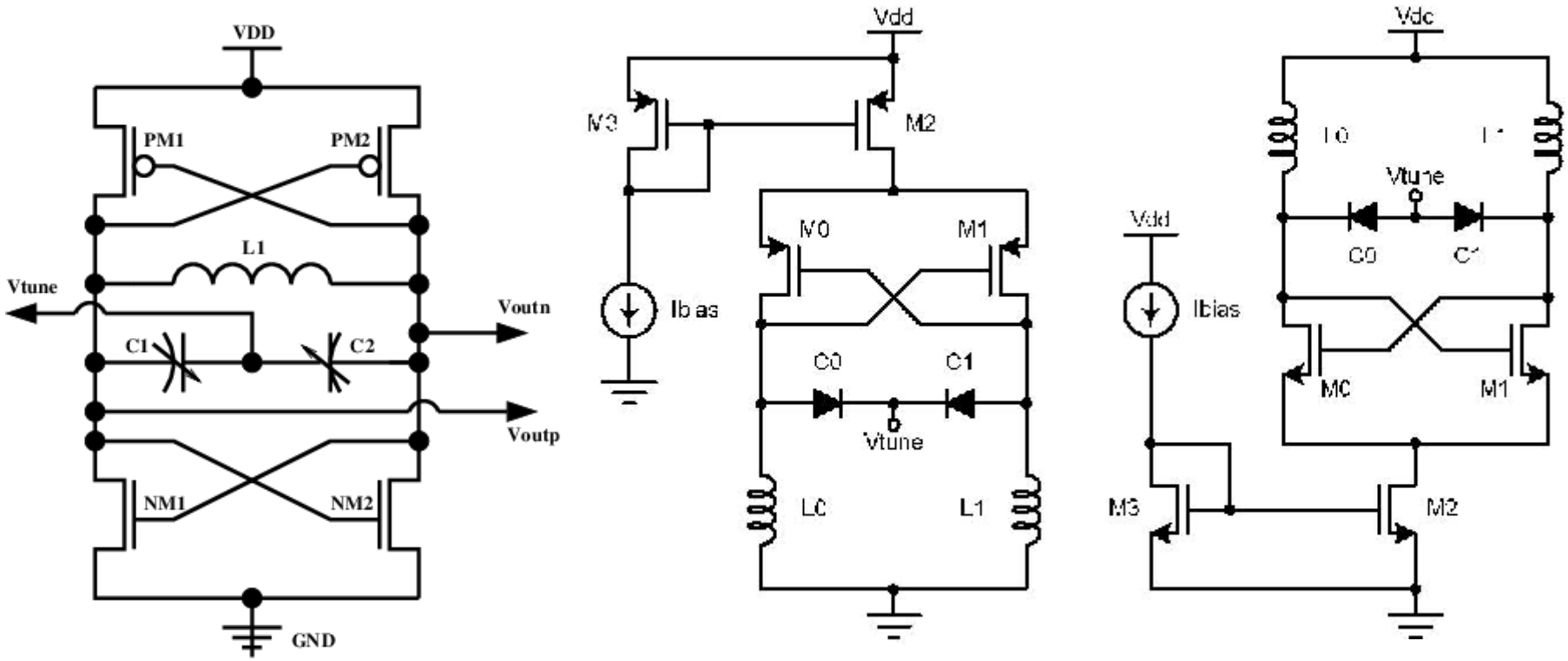
Varactor design: some design consideration





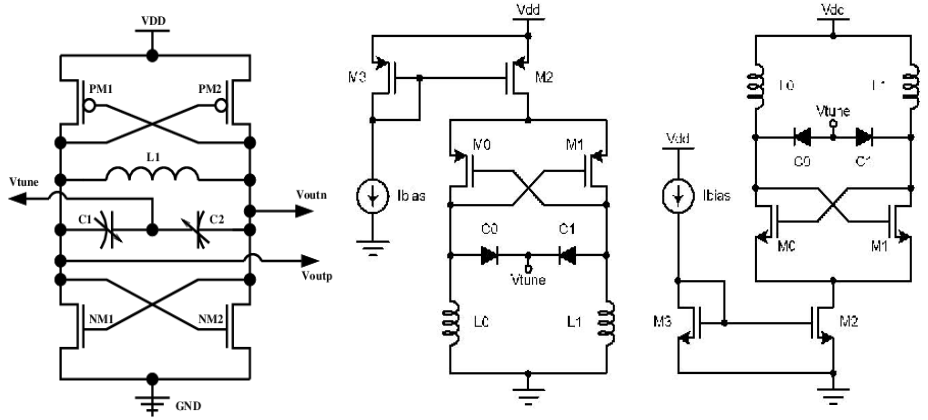
- Kvco is chosen based on several factors:
  - Whether system is required to stay locked over temp (for example TV)
  - Phase noise target
  - PLL design
- A “tune voltage” monitor circuit (simple comparator circuit) is usually needed to ensure the varactor tune voltage remains within the compliance range of the PLL charge pump. If it falls out of that, a cap-bank selection routine is triggered to move to the next cap bank.

Active circuit selection:



- There are various active VCO circuit topologies, such as nmos, pmos and cmos. The above topologies are just a small example of the so many varieties available.

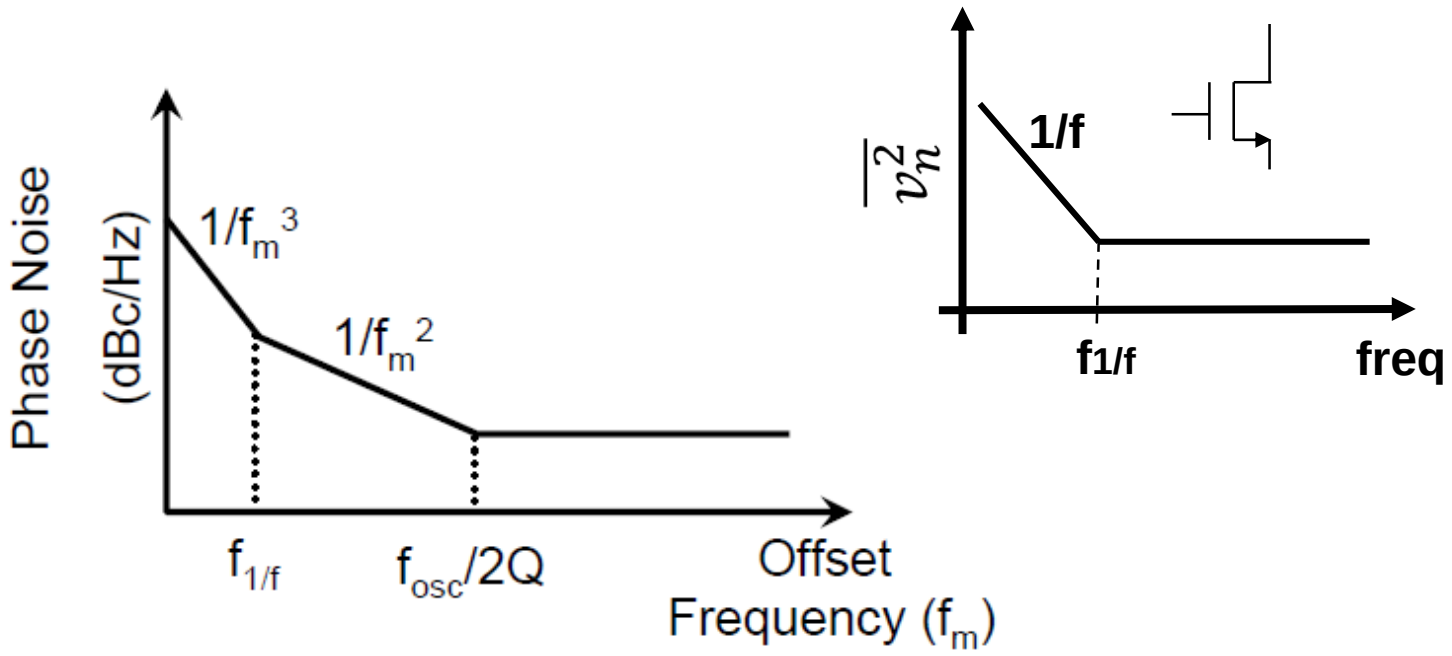
Active circuit selection: merits of each topology



Each has its own merits and shortcomings:

- **NMOS** VCO has the advantage of swinging above Vdd (pk-pk swing can be ~4xVdd differential). However nmos device are known to have large flicker noise
- **PMOS** VCO has same advantage as nmos in terms of swing. It has also lower flicker noise than nmos. It has the disadvantage that pmos has 2~3x lower mobility than nmos (bulk process) and so larger device is needed for same current and this result in increasing the Cfix of the tank which lowers Q (need lower inductor to achieve resonance). In FinFet process pmos and nmos devices have almost same mobility, so pmos can be better there
- **CMOS** VCO has the advantage of offering twice gm for same current due to current reuse. However, it suffers a swing limit. They are useful in relaxed phase noise requirement, VCO with higher V_{dd} or VCOs operating in the current-limiting regime

Device noise and its relation to phase noise



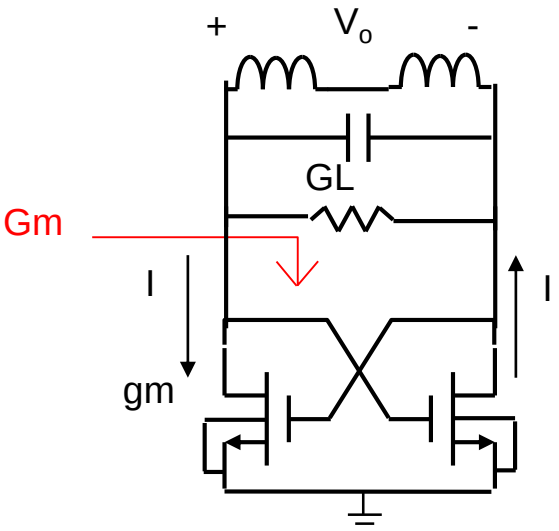
- The device flicker noise corner directly impacts the phase noise $1/f^3$ region.
- Phase noise decays by 20dB per decade in the $1/f^2$ region
- Device sizing and biasing is key to manipulate these regions

Optimum device biasing

At DC (start of oscillation), Gm of active device is:

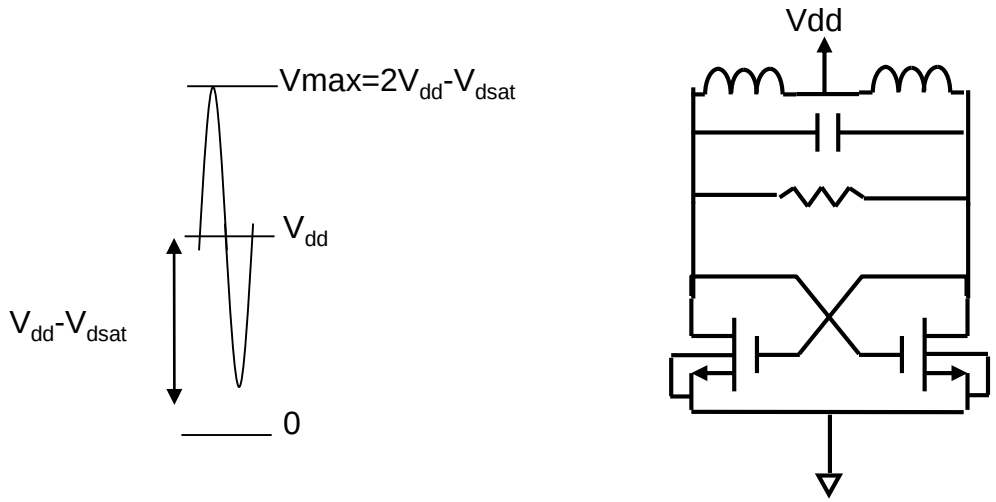
$$G_m = -g_m / 2$$

In order to ensure startup:
$-G_m$ must be > G_L (loss of the tank)



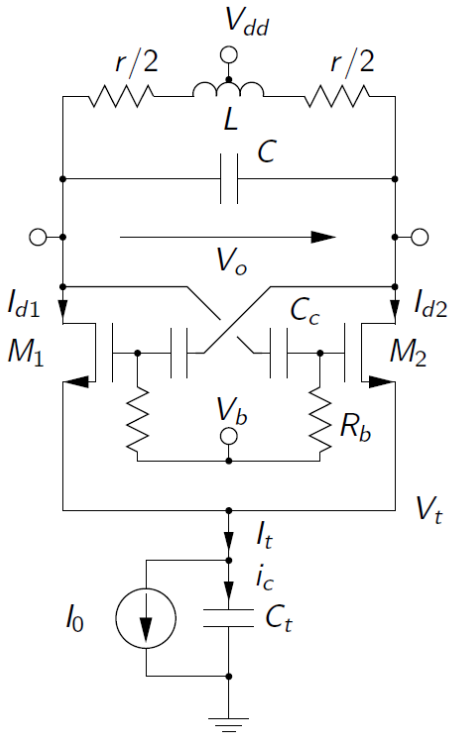
- A good ratio of $|G_m|/G_L$ is ~2. A lower value (close to 1 but still >1) could result in the risk of VCO not starting up due to other unaccounted for losses in the circuit. However a much larger ratio can result in larger than necessary device size, which can degrade phase noise due to much more none-linear G_m vs swing and more none-linear device cap AM to PM)
- Please note the G_L is frequency dependent. Therefore, G_m needs to be chosen to guarantee oscillation at the worst case value of G_L over freq.
- G_m is likely to be temperature/process dependent, therefore the $|G_m|/G_L$ ratio needs to be checked over PVT (and frequency)
- As we discussed earlier large-signal G_m is a function of V_o. Its absolute average value over V_o (steady state) equals to G_L.

Selecting optimum VCO core supply voltage:



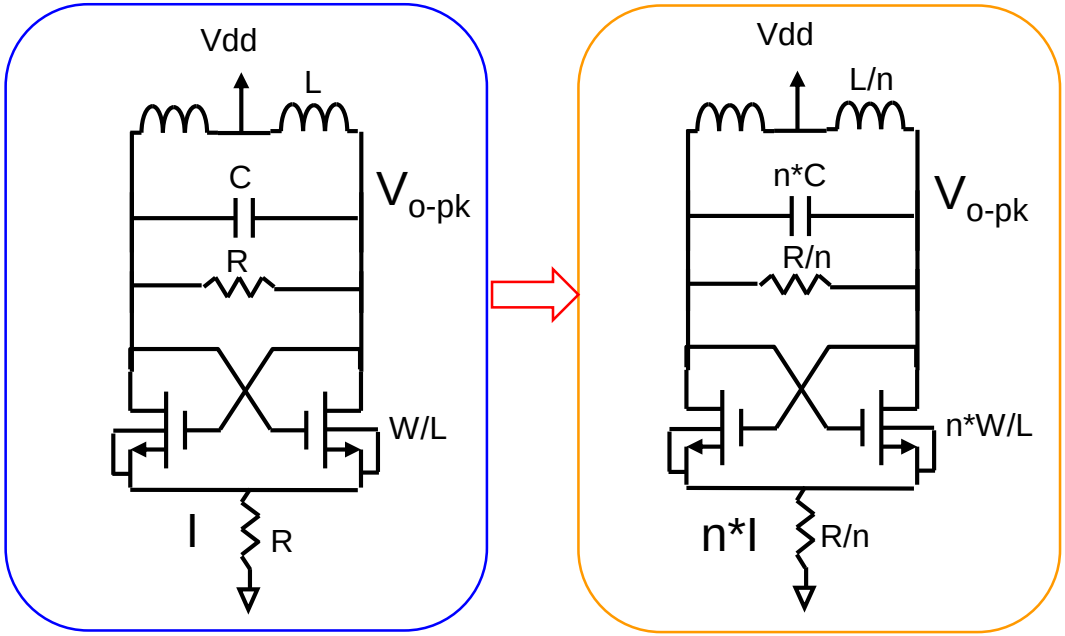
- In order to improve phase noise, we need to maximize the VCO swing across the tank per the Leeson's formula
- However, active circuit transistors experience both HCI and NCS stress under large swing.
- Need to get the maximum rating of transistors and from that decide the VCO internal Vdd.
- For example, assume I/O NMOS Vmax=4.2V (set by NCS). With Vdsat of 0.1V, Vdd can then be calculated to be 2.15V

AC coupling active device to tank:



- AC coupling active circuit to tank allows you to:
  - Reduce swing at gate-source of active devices for better reliability (in case device-oxide breakdown voltage limits VCO swing without it)
  - Chose Vb to control the initial-bias point of active devices relative to their size (class-C VCO), which can be useful to lower phase noise (sometimes)

How much bias current we need:

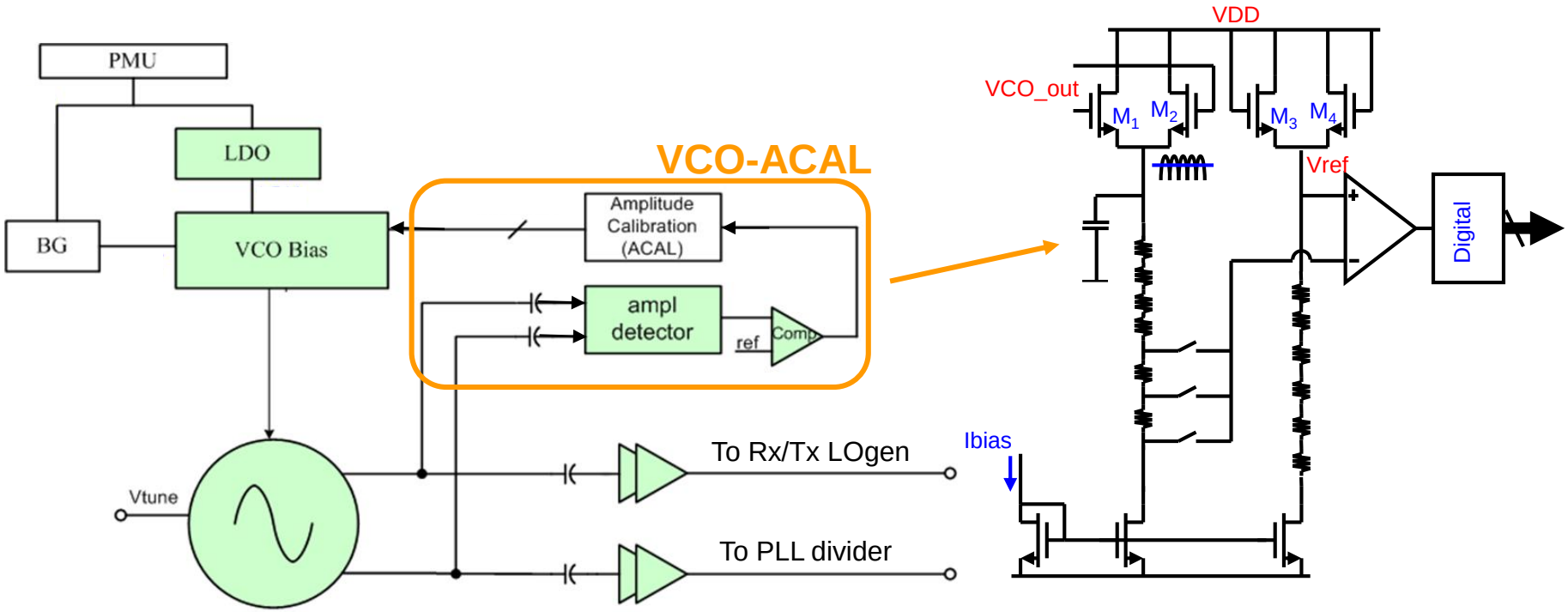


- Initial design, sweep W/L of active device to get $|G_m|/G_L$ to your target (say 2), which is best kept between the current limiting and voltage limiting regimes
- If $L(f_{off})$ does not meet requirement, increasing current is your last resort to improve phase noise. Increase current by scaling circuit elements by n:

All C → nC, L → L/n, W → nW (as result, tank loss scales also R → R/n)

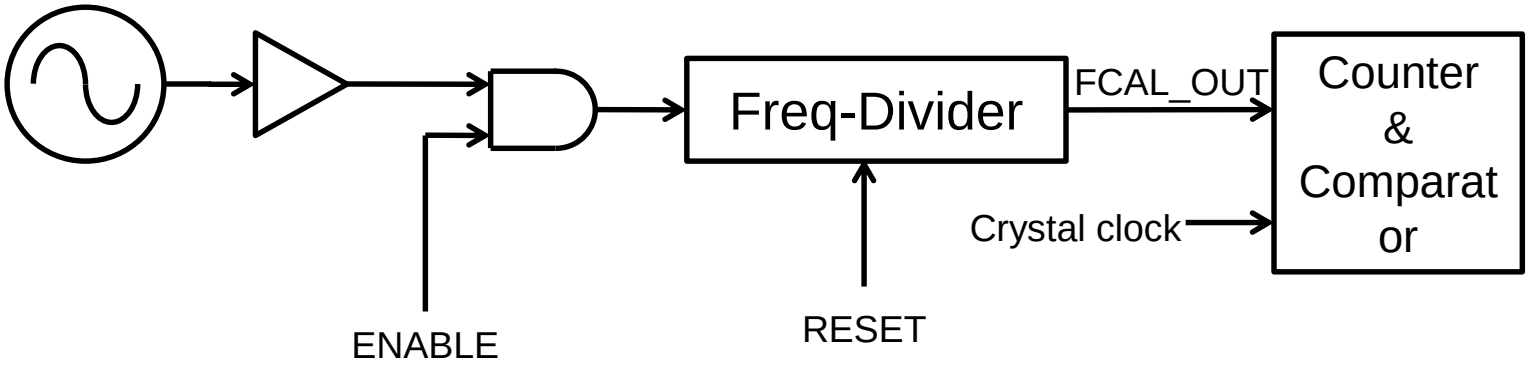
- Output swing $V_{o\text{-}pk}$, and tank Q will be kept constant
- $L(f_{off})$ improves by 10log(n)

VCO Amplitude Calibration: ACAL



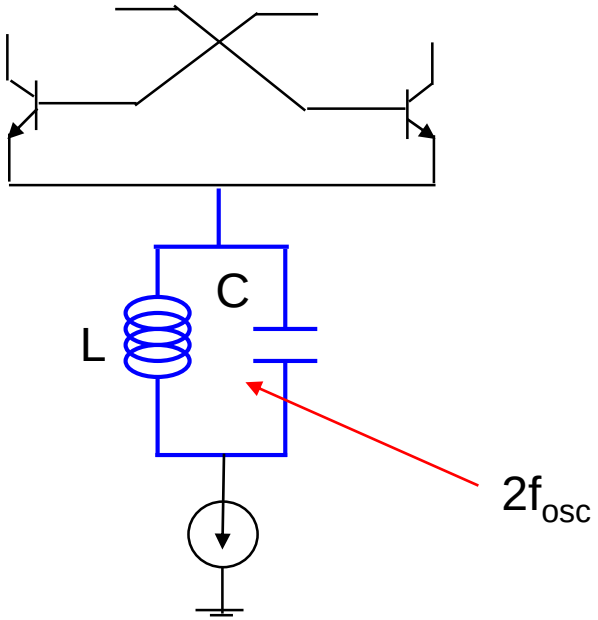
- VCO output swing changes over PVT and also over frequency.
- VCO phase noise is inversely proportional to the square of VCO amplitude swing → keep VCO swing relatively constant over such variations
- A VCO amplitude calibration circuit converts VCO swing to DC and compares it to a DC reference. VCO current is adjusted till target VCO amplitude is met.

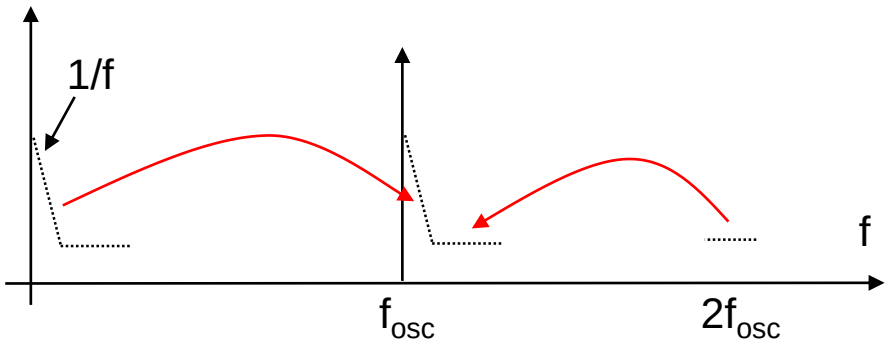
VCO Cap-bank Frequency Calibration: FCAL



- VCO cap-bank frequency coverage range is calibrated upon power-on so proper cap-bank is selected when channel switching for fast PLL locking
- For each cap-bank, VCO output frequency is divided by a cal-divider. A digital counter compares counted divided VCO clocks to that from a crystal reference and so calculates the VCO frequency.
- Vtune is set to middle-point during FCAL. However, FCAL can be repeated at the min/max Vtune to ensure frequency coverage.
- FCAL values are stored in chip memory. When a channel is selected, the correct cap-bank that gives closest target frequency is selected and PLL is then engaged

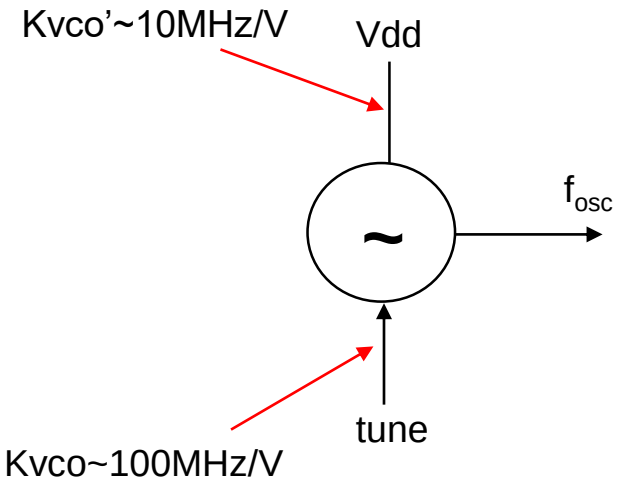
Phase noise due to noise at twice f_{osc}:





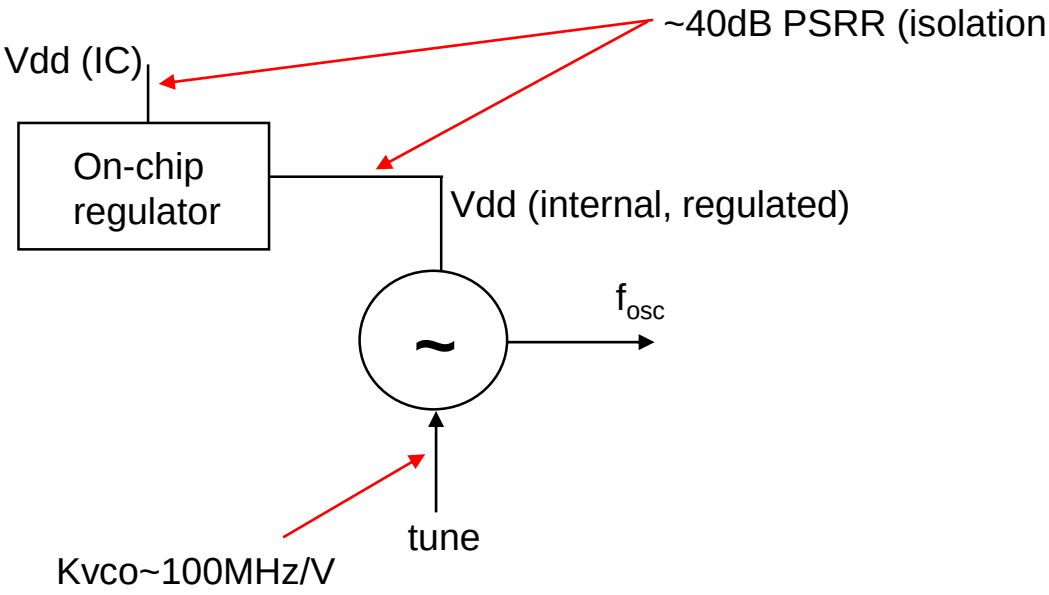
- The tank resonates at twice the the oscillation frequency to block bias noise at $2f_{osc}$ from getting down converted to $f_{osc.}$. A 1.5~2dB improvement in phase noise can be observed

VCO Bias and supply pushing:



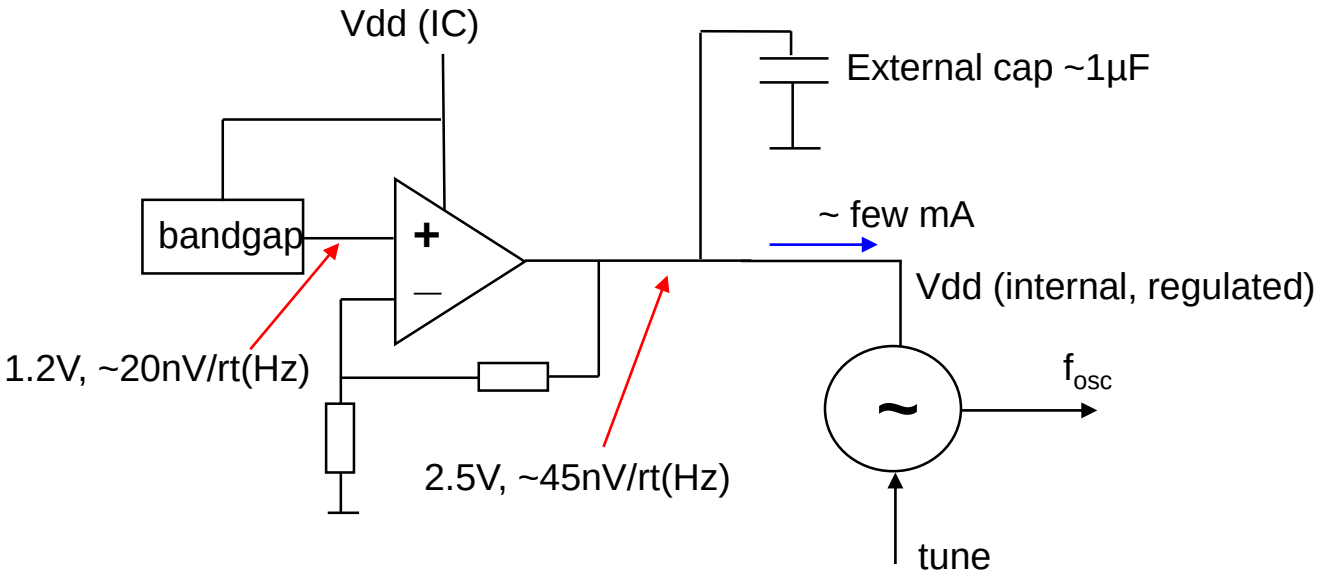
A VCO is a highly sensitive block to any disturbance at any of its internal nodes (not only the tune port). Therefore, each internal node of the VCO circuit has its own "parasitic" Kvco, by which any voltage disturbance on that node gets translated into a shift or disturbance to the oscillation frequency. The two most important nodes being V_{dd} and ground, since they connect the VCO to the outside world, and therefore are more prone to disturbance. In fact, for a 100MHz Kvco cross coupled 2GHz VCO, the parasitic Kvco at the V_{dd} line is <1MHz/V (<~one tenth of the main Kvco).

Reducing VCO supply pushing:



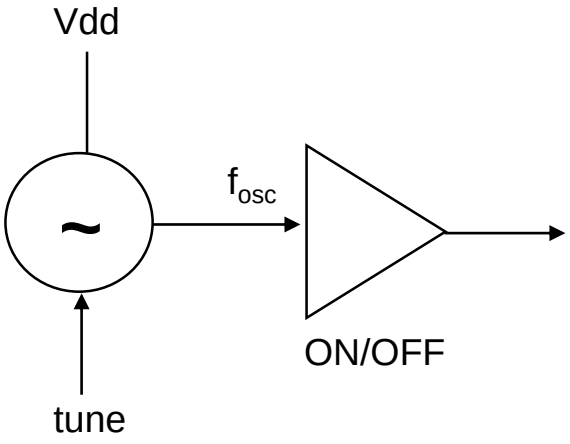
To reduce supply pushing (parasitic Kvco at the supply port of the VCO), an on-chip regulator is used to regulate the VCO supply. A typical regulator has ~40dB PSSR up to few 10MHz. This means a 100mV disturbance at the Vdd line of the IC results in only 1mV disturbance at the regulated VCO Vdd. With 10MHz/V Kvco at the Vdd line of the VCO, this translates into 10kHz shift in the VCO frequency. Without the regulator, the shift is 1MHz. In some application, such as WLAN, the supply pushing of a VCO is a big concern to satisfy the Tx/Rx turn around time of 10µs max. Note that any VCO disturbance will settle after a time set by the PLL settling time. Please note that if Vdd (IC) comes from DC-DC converter, the regulator PSRR is chosen so that the spur due DC-DC ripple clock is below target (set by in-band SNR or out of band emission or both)

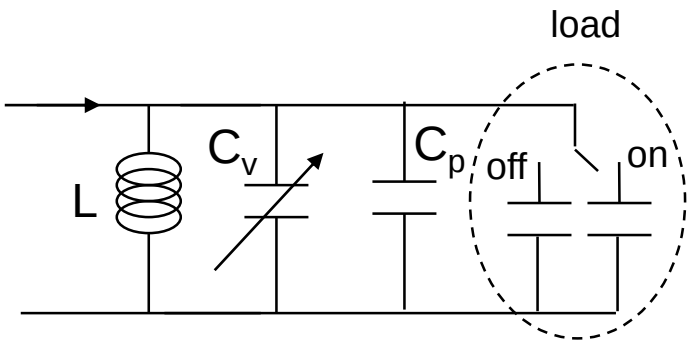
A typical VCO supply regulator:



A very stable reference is generated on chip that is supply independent (bandgap). This voltage is multiplied up by a process independent gain stage with good power supply rejection. Note that the output stage of the opamp above needs to supply few mA of VCO current while having only 0.2V on its output device (Vdd min is 2.7V and Vreg is 2.5V). Bandgap references are noisy in general. A typical 100uA bandgap has a 20~30nv/rt(Hz) noise. This noise gets multiplied up by the opamp circuit. Since the VCO core is biased from this reference, the low frequency noise of this regulator gets upconverted to phase noise. An external cap sometimes is used to limit the regulator noise bandwidth beyond the PLL loop filter corner frequency where there in no rejection from PLL. An alternative is to add a large RC filter at the bandgap port of the regulator to filter out the bandgap noise (in this case, perhaps on-chip cap at regulator output is enough)

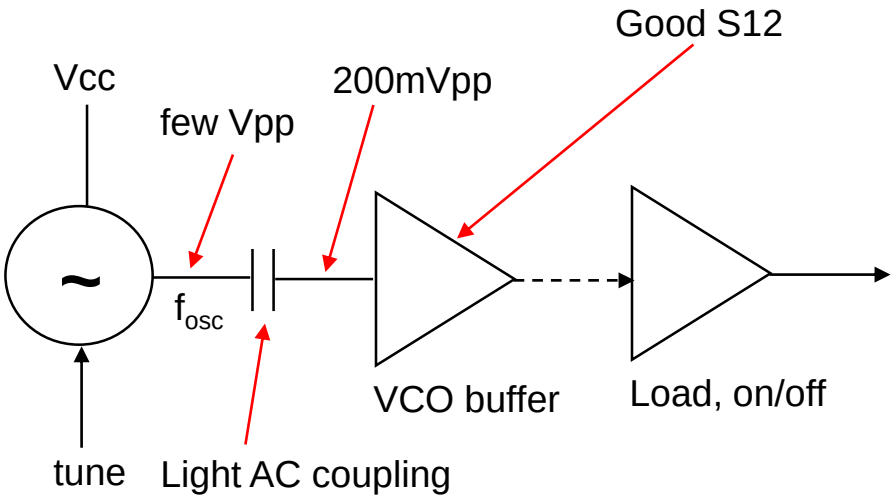
VCO load pulling:





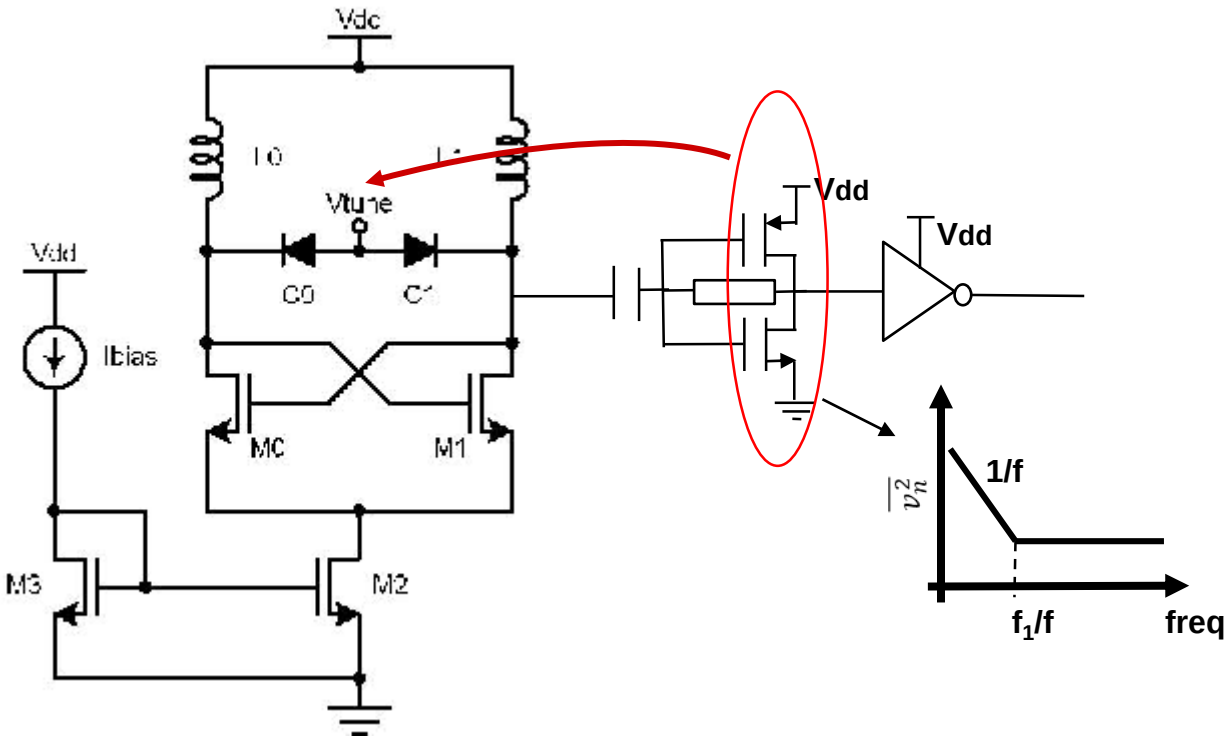
VCO load pulling is specified as a peak-peak change in the oscillation frequency as the load of the VCO is turned on and off. The equivalent input capacitance of the load changes when the load is switched on and off. This changes the effective capacitance loading to the VCO tank shifting its oscillation frequency. This is particularly important in cellular systems when mixers with multi-modes has to change gain. Also in wireless TDD systems (WLAN, GSM) where the Rx and Tx are toggled on and off while the PLL is kept locked at one frequency.

Minimizing VCO load pulling and buffer kick back



A VCO buffer with good S12 is used (perhaps cascode) to isolate the load from the VCO. Note that the buffer remains on as long as the VCO is on, and is considered part of the VCO. In addition, the output of the VCO is lightly AC coupled to the buffer via a small AC coupling cap. The cap blocks the flicker noise of buffer devices from leaking back to VCO tank. This arrangement creates a capacitive voltage divider between the buffer input capacitance and that of the AC coupling cap. This divide ratio can be as high as 20dB since the voltage swing at the VCO output is few volts while the VCO-buffer needs only few hundred mV at its input. Therefore, the total load to VCO isolation equals S12 plus the voltage divide value, which is close to 50dB total for a good design.

VCO buffer noise kick back to VCO tank:



Phase noise of buffer can kick back to VCO impacting its phase noise via two mechanisms. First the large flicker noise of the small VCO buffer circuit devices leak back to VCO tank and get upconverted to VCO frequency. Second, the buffer own phase noise leaks back to VCO via finite buffer to VCO-tank isolation. Therefore, it is important to lightly-couple the VCO buffer to VCO tank to reduce this effect as discussed earlier. In addition, buffer flicker noise needs to be well designed.

References:

[1] D. Ham, A. Hajimiri, " Concepts and Methods in Optimization of Integrated LC VCOs," IEEE JSSC, Vol. 36, No. 6, June 2001, pp. 896-909

[2] P. Andreani, S. Mattisson, " On the Use of MOS Varactors in RF VCOs," IEEE JSSC, Vol. 35, No. 6, June 2000, pp. 905-910

[3] D. Leason, " a Simple Model of Feedback Oscillator Noise Spectrum," *in Proc. IEEE*, February 1966, pp. 329-330.

[4] J. Rael, A. Abidi, " Physical Processes of Phase Noise in Differential Oscillators," *in Proc. IEEE CICC 2000*, pp. 569-672.

[5] A. Hajimiri, T. Lee, "Oscillator Phase Noise: A Tutorial," IEEE JSSC, Vol. 35, No. 3, March 2000, pp. 326-336

[6] J. Craninckx, *et. al*., "A 1.8-GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors," IEEE JSSC, Vol. 32, No. 5, May 1997, pp. 736-744

[7] Andrea Mazzanti, *et. al*., "Class-C Harmonic CMOS VCOs, With a General Result on Phase Noise," IEEE JSSC, Vol. 43, No. 12, December 2008, pp. 2716-2729

[8] E. Hegazi, H. Sjoland and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," IEEE JSSC vol. 36, no. 12, Dec. 2001, pp. 1921-1930.

[9] F. Pepe, *et. al*., "Suppression of Flicker Noise Up-Conversion in a 65-nm CMOS VCO in the 3.0-to-3.6 GHz Band," IEEE JSSC vol. 48, no. 10, Oct. 2013, pp. 2375-2389.