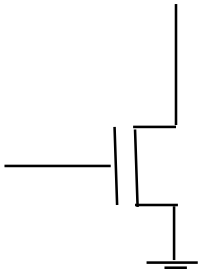
CMOS RF LNA Design

- **CMOS LNA Design**
  - Noise sources in CMOS device at RF
  - NF_{min} and $Z_{S\text{-}opt}$ for an NMOS
  - Simultaneous noise and power match
  - LNA design under supply power constraint
- **References**

CMOS LNA Design:

Noise sources in a common-source nmos device:



1. Drain current channel thermal noise

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\gamma g_{d0}$$

Where g_{do} is the g_{do} is the zero bias drain conductance, and γ is a bias dependent factor that, for long channel devices, ranges from 2/3 to 1. However, γ can be as large as 2 or 3 for short channel devices.

2. thermal noise of the gate poly resistance

$$\frac{\overline{v_g^2}}{\Delta f} = 4kTR_g$$

The silicide poly of the gate acts as a resistor in series with the gate with thermal noise power. The gate resistance, R_g, can be reduced by using a multi-finger configuration. In this Case. R_g can be written as a function of device size and number of fingers as:

$$R_g = \frac{R_{sh}W}{3n^2L}$$

Where *W*, *L* are the device width and length, respectively. R_{sh} is the gate poly sheet resistance, and *n* is the number of gate fingers. The 1/3 factor assumes each gate finger is contacted only at one end. If each finger is contacted at both ends, the factor becomes 1/12.

3. Thermal noise of the bulk resistance appearing on drain due to backgate transconductance, g_{mb}:

$$\frac{\overline{i_d^2}}{\Delta f} = 4kTg_{mb}^2 R_{blk}$$

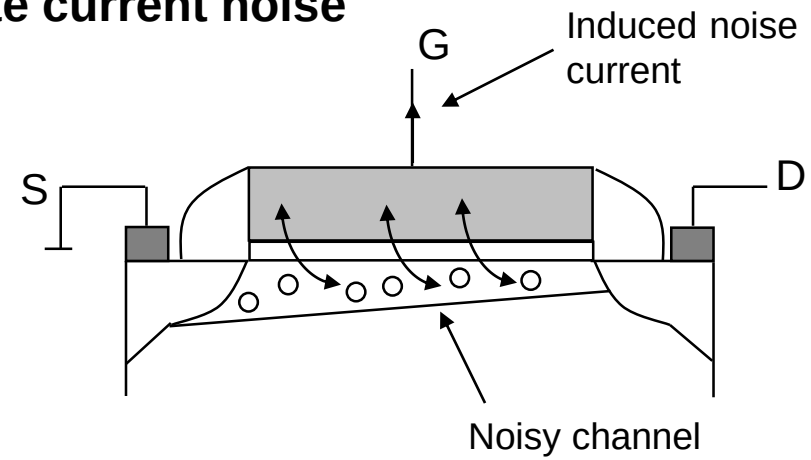
The backgate epitaxial resistance can be modeled as a resistor in series with the device bulk terminal. There is a noise voltage associated with this resistance, which produces a drain current noise due to the backgate g_{mb}.

For CMOS technologies designed for RF application, the ratio of the drain current noise due bulk resistance to that due to channel thermal noise is in the range of:

$$0.05 \leq \frac{g_{mb}^2 R_{blk}}{g_{d0}} \leq 0.2$$

The bulk resistance is highly layout dependent and can be highly reduced by placing the substrate contacts very close to the device. Thus, the effect becomes of secondary importance and can be ignored in noise calculations, as we will do in the analysis to follow.

4. Induced gate current noise



$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta g_g$$

The fluctuating carriers inside the noisy channel capacitively couples to the gate
Through the gate oxide inducing a noise current at the gate. The value g_g is given by

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}}$$

The coefficient δ of the gate noise equals to 4/3 for long channel devices.

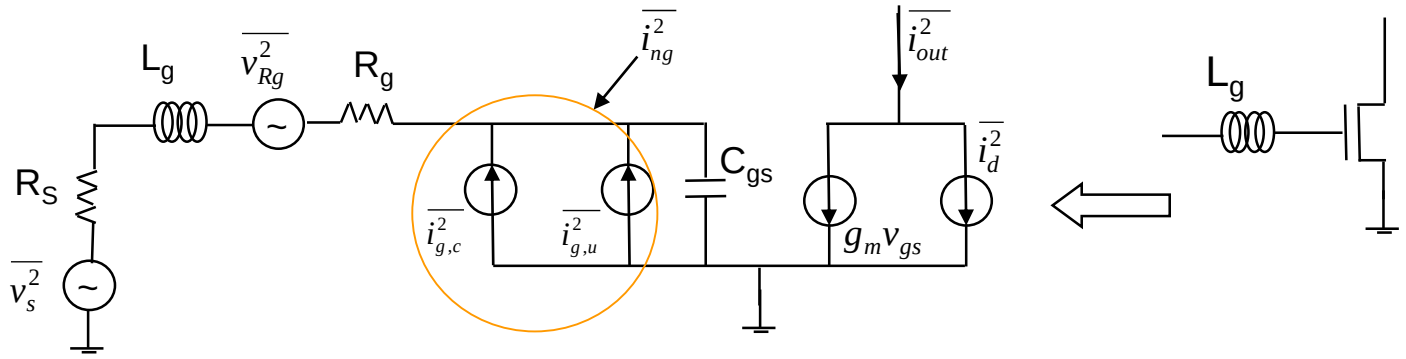
The induced gate noise and the drain thermal noise are partially correlated. The correlation factor is given by

$$|c| = \left| \frac{\overline{i_g i_d}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}} \right| \approx 0.395$$

The 0.395 value is for long channel devices. Note that the value of c = j0.395 indicates the capacitive coupling nature of gate noise. The gate noise then can be written as the sum of two components: one is correlated with the drain thermal noise, and the other component is totally uncorrelated, as follows

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta g_g \left(1 - |c|^2\right) + 4kT\delta g_g |c|^2$$

I. CS NMOS noise model without degenertion:



Applying the 2-port noise theory to the above circuit, after elaborate math (R_g and C_{gd} are ignored), one can get:

$$F(Y_S) = F_{\min} + \frac{R_n}{G_S}\left[(G_S - G_{S-opt})^2 + (B_S - B_{S-opt})^2\right]$$

where $R_n^I = \frac{\gamma}{\alpha}\frac{1}{g_m}$ and so $v_n = 4kTR_n^I\Delta f$

$$Y_{S-opt}^I = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}\left(1-|c|^2\right)} - sC_{gs}\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right), \text{ where } \alpha = \frac{g_m}{g_{d0}}$$

$$F_{\min}^I = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)}, \text{ where } \omega_T = \frac{g_m}{C_{gs}}$$

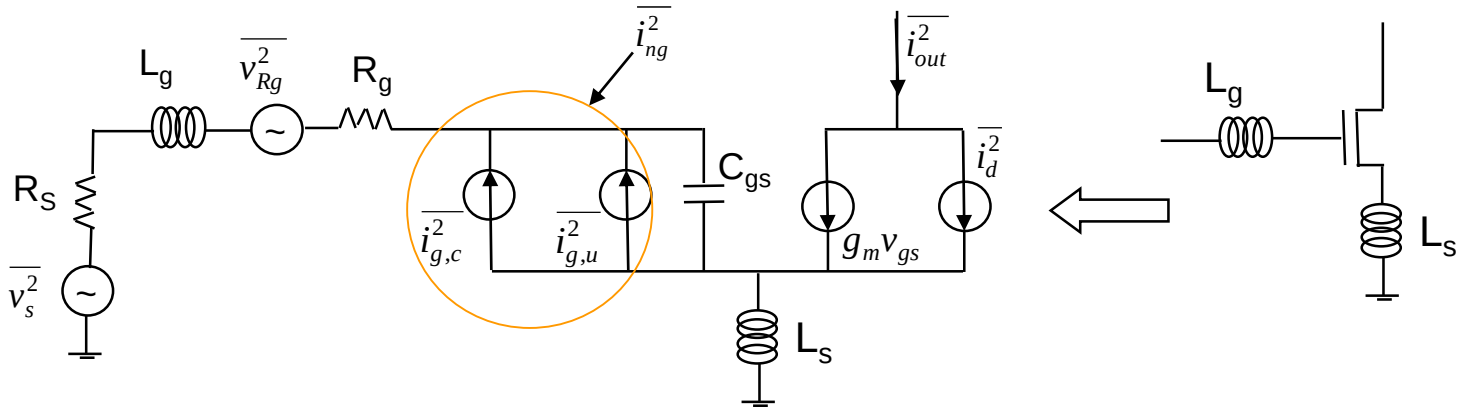
The input admittance to the CS circuit is given by:

$$Y_{in}^{I} = sC_{gs}$$

Which is totally capacitive. Note that the gate resistor has been neglected in the analysis. Also the gate-drain capacitance is also neglected, because we assume a cascode topology.

In order to achieve minimum noise figure the device has to be matched to the optimum noise admittance (impedance). It is clear that the optimum noise admittance and the input admittance to this LNA are inherently different, making simultaneous NF and power match impossible.

II. CS NMOS with inductive degeneration:



$$R_n^{II} = R_n^I = \frac{\gamma}{\alpha}\frac{1}{g_m} \quad \text{, where } \alpha = \frac{g_m}{g_{d0}}$$

$$Z_{opt}^{II} = Z_{opt}^{I} - sL_s$$

$$F_{\min}^{II} = F_{\min}^{I} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)} \text{ , where } \omega_T = \frac{g_m}{C_{gs}}$$

note that the optimum noise impedance is given by:

$$Z_{opt}^{I} = \frac{1}{Y_{opt}^{I}} = \frac{\sqrt{\frac{\alpha^2\delta(1-|c|^2)}{5\gamma}} + j\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\frac{\alpha^2\delta(1-|c|^2)}{5\gamma} + \left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}}$$

The input impedance to the CS circuit with inductive degeneration is given by:

$$Z_{in}^{II} = \omega_T L_s + \frac{1}{sC_{gs}} + sL_s$$

It is interesting to note that the inductive degeneration did not affect the minimum NF of the CS device nor the equivalent noise resistance. What it really did is to shift the optimum noise impedance. Furthermore, it created a real part in the input impedance to the device, therefore, help reduce the discrepancy between Z_{opt} and Z_{in} of the LNA.

In order to give insight, the optimum noise impedance can be rewritten as:

$$Z_{opt}^{II} = \mathrm{Re}\left[Z_{opt}^{I}\right] - m\frac{1}{sC_{gs}} - sL_s$$

For long channel device, the value of m≈0.6. With technology scaling, the ratio of δ/γ gets closer to 2, α becomes a bit less than 1, and *c* is slightly gets higher than 0.4 (for 0.25μ CMOS, *c* = 0.5). Therefore, m gets closer to unity with technology scaling. Therefore. Inductive degeneration helps bring Z_{opt} closer to Z_{in}, which could facilitate simultaneous noise and power match as will be seen next.

In order to achieve power match, the following condition must be met:

$$Z_{in} = Z_s^* \quad \text{; wich means}$$
$$\mathrm{Re}[Z_{in}] = \mathrm{Re}[Z_s]$$
$$\mathrm{Im}[Z_{in}] = -\mathrm{Im}[Z_s]$$

In order to achieve minimum NF, the following condition must be met:

$$Z_{opt} = Z_s \quad \text{; wich means}$$
$$\mathrm{Re}[Z_{opt}] = \mathrm{Re}[Z_s]$$
$$\mathrm{Im}[Z_{opt}] = \mathrm{Im}[Z_s]$$

With technology scaling, we can assume that the following condition is always satisfied (m=1):

$$\mathrm{Im}[Z_{in}] = -\mathrm{Im}[Z_{opt}]$$

Minimum channel length is used to maximize ω_T. As a result, one need only to solve for device width **W** (to set C_{gs}), $\mathbf{V_{gs}}$ to set ω_T, and $\mathbf{L_s}$. Therefore the above 3 equations are enough to solve for these 3 unknowns at a given Zs, as follows.

Design procedure for simultaneous NF and power match:

● $\mathrm{Re}[Z_{opt}]$ depends only on the device C_{gs}, for a given technology at a given frequency. C_{gs} is set by device width, W, assuming min channel length device. Therefore, chose W to set $\mathrm{Re}[Z_{opt}] = \mathrm{Re}[Z_s]$. This step will set the device size.

$$\mathrm{Re}[Z_{opt}^{II}] = \mathrm{Re}[Z_{opt}^{I}] = \frac{\sqrt{\frac{\alpha^2\delta(1-|c|^2)}{5\gamma}}}{\omega C_{gs}\left\{\frac{\alpha^2\delta(1-|c|^2)}{5\gamma} + \left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} = \mathrm{Re}[Z_s]$$

● $\mathrm{Im}[Z_{opt}]$ depends on degeneration inductor, L_s, for a given device size and frequency. Chose L_s to set $\mathrm{Im}[Z_{opt}] = \mathrm{Im}[Z_s]$. This will also automatically set $\mathrm{Im}[Z_s] = -\mathrm{Im}[Z_{in}]$. This step sets the value of degeneration inductor L_s.

$$\mathrm{Im}[Z_{opt}^{II}] = \frac{\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\frac{\alpha^2\delta(1-|c|^2)}{5\gamma} + \left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} - \omega L_s = m\frac{1}{\omega C_{gs}} - \omega L_s = \mathrm{Im}[Z_s] = -\mathrm{Im}[Z_{in}]$$

● Finally, Re[Z_{in}] depends on device ω_T for a given degeneration L_s. Moreover ω_T depends on device g_m, which depends on device V_{gs} for a given device size W. Therefore, set device V_{gs} (hence bias current I_{dd}) to set Re[Z_{in}] = Re[Z_s].

$$\mathrm{Re}[Z_{in}] = \omega_T L_s = \frac{g_m}{C_{gs}} L_s$$

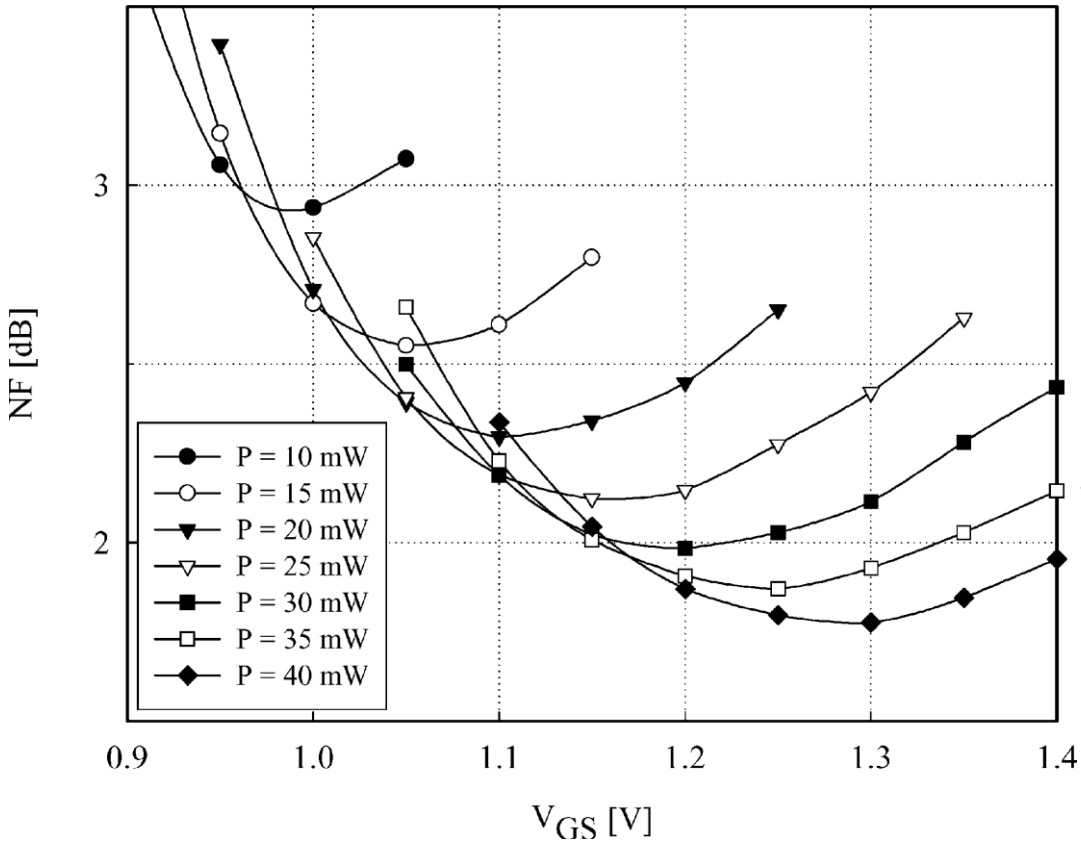
Following the three steps above results in an LNA that achieves minimum NF with simultaneous NF and power match.

Note that the matching network is considered part of the source impedance, Z_s. This could be as simple as an inductor in series with the device gate, L_g, as shown.

It is important to note that the above design procedure assumes the current consumption is flexible. In other words, the methodology guarantees minimum NF, with simultaneous NF and power match without any consideration or limits to power dissipation. In some wireless systems, this is not desirable, and therefore we will discuss next two other design procedures for power constraint designs.

Limitations of the derived equations:

As seen from equations, as device size gets small due to limitation on power consumption of LNA (small W) and/or low operating frequency, the value of degeneration inductor, L_s, needed to provide noise/power match becomes quite large. This results in LNA gain drop (low gm) and so increase in NF. You will start to see in simulation that NFmin degrades as a function of increasing Ls (because some neglected parameters like Cgd start to come into play)

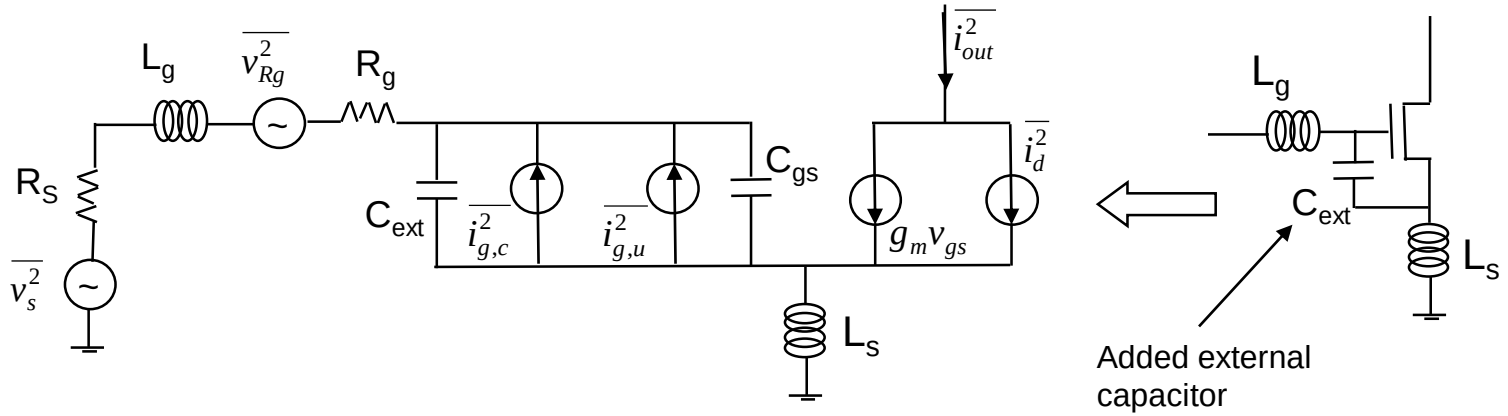


Simulated NF of inductively degenerated LNA as a function of device Vgs and W for given power consumption of LNA. Notice how for each curve there exists a device width that leads to optimum NF [1]:

$$W_{opt} \approx \frac{1}{3\omega C_{ox} R_s Q_{in,opt}}, \quad Q_{in,opt} = |c|\sqrt{\frac{5\gamma}{\delta}}\left[1+\sqrt{1+\frac{3}{|c|^2}\left(1+\frac{\delta}{5\gamma}\right)}\right]$$

$$F_{\min}^{P} \approx 1 + 2.4\frac{\gamma}{\alpha}\left(\frac{\omega}{\omega_T}\right)$$

III. CS NMOS with simultaneous NF and power match under power constraint:



For the small signal circuit of the new LNA, new sets of equation emerge:

$$\overline{i_{ng}^2} = 4kT\delta_{eff}\frac{\omega^2 C_t^2}{5g_{d0}}\Delta f \quad \text{where} \quad \delta_{eff} = \delta\left(\frac{C_{gs}}{C_t}\right)^2 \text{ and } C_t = C_{gs} + C_{ext} \;\; ; \;\; R_n^{III} = R_n^I = \frac{\gamma}{\alpha}\frac{1}{g_m}$$

$$Z_{opt}^{III} = \frac{\sqrt{\frac{\alpha^2\delta(1-|c|^2)}{5\gamma}} + j\left(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\frac{\alpha^2\delta(1-|c|^2)}{5\gamma} + \left(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} - j\omega L_s$$

$$F_{\min}^{III} = F_{\min}^{I} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)}$$

It is interesting to note that the addition of C_{ext} did not affect F_{min} or R_n. What it did is shifting the value of Z_{opt}.

$$Z_{in}^{III} = \frac{g_m L_s}{C_t} + \frac{1}{sC_t} + sL_s$$

In order to achieve simultaneous NF and power match, the following conditions must be met:

$$\mathrm{Re}[Z_s] = \mathrm{Re}[Z_{opt}] = \frac{\sqrt{\frac{\alpha^2\delta(1-|c|^2)}{5\gamma}}}{\omega C_{gs}\left\{\frac{\alpha^2\delta(1-|c|^2)}{5\gamma} + \left(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}}$$

$$\mathrm{Im}[Z_s] = \mathrm{Im}[Z_{opt}] = \frac{j\left(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\frac{\alpha^2\delta(1-|c|^2)}{5\gamma} + \left(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} - j\omega L_s$$

$$\mathrm{Re}[Z_s] = \mathrm{Re}[Z_{in}] = \frac{g_m L_s}{C_t} \quad ; \text{and} \quad \mathrm{Im}[Z_s] = -\mathrm{Im}[Z_{in}] = \frac{1}{\omega C_t} - \omega L_s$$

As discussed earlier, with technology scaling, Im[Z_{in}] gets closer to Im[Z_{opt}]. Therefore, one needs to solve for device size, W, V_{gs}, C_{ext} and L_s. There are 3 equations to solve these 4 unknowns. As a result, one needs to set one variable (power consumption in this case) and solve for the remaining 3 variables.

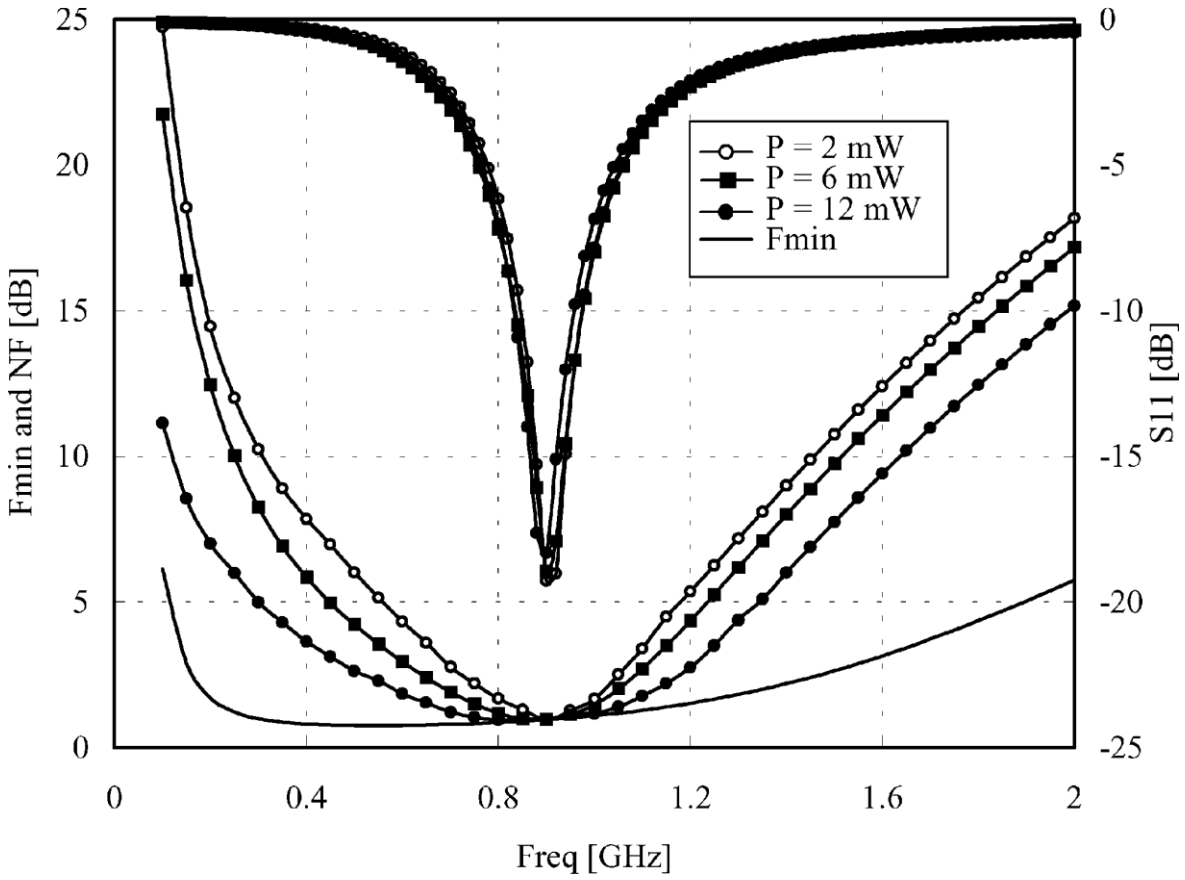
Since Re[Z_{in}]=Re[Z_{opt}]=Re[Z_s], one can find

$$L_s \approx \frac{\sqrt{\frac{\alpha^2 \delta (1-|c|^2)}{5\gamma}}}{\omega \omega_T C_t}$$

It is clear that the added external capacitor helps reduce the required value of L_s to achieve simultaneous NF and power match. Note that C_{ext} results in a drop of the available gain due to drop of the device effective cutoff frequency. For example, if C_{ext}=1.5C_{gs}, the gain drops by almost 1dB at 900MHz for 0.25µ CMOS [2].

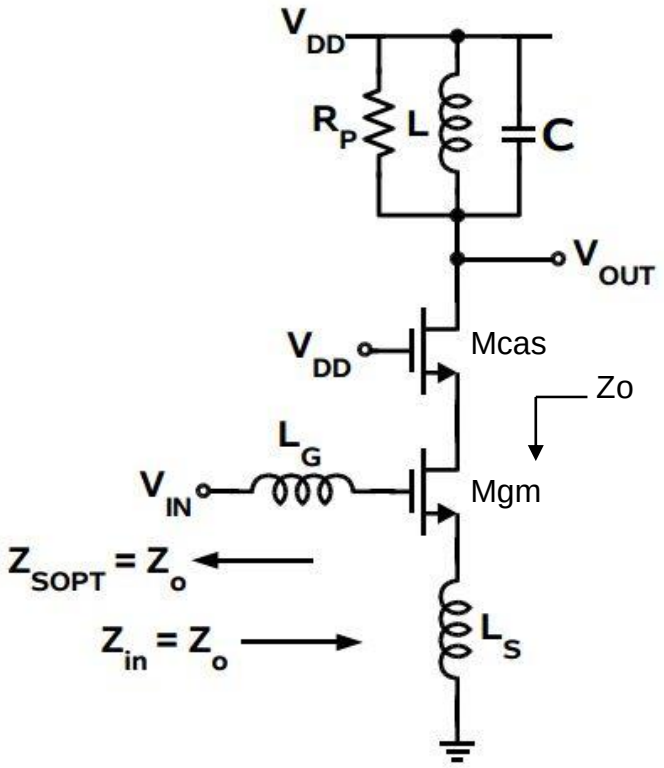
The design flow qualitatively is then as follows:

- chose V_{gs} that results in achieving NF_{min}. Note that NF_{min} depends on ω_T, which can be written as a function of V_{gs} and independent on W.
- chose device W to meet the power constraint for a given V_{gs}.
- find L_s and C_{ext} values that sets Z_s=Z_{opt}, and Re[Z_s]=Re[Z_{in}].



An example of LNA NF for different power consumption constraints (0.25u CMOS @900MHz). Note how NF touches NFmin at 900MHz. NF rises quickly when deviating from optimum point due to higher noise resistance for lower power consumption of LNA (lower G_m and f_T).

Completing the cascode LNA circuit:



Cascode device does not contribute to LNA NF if properly sized
Because of high Zo of Mgm, drain noise of Mcas flows into its own source gate:

$$V_{gs\_cas} = -i_{dn} \times \frac{1}{g_m + sC_{gs\_cas}}$$

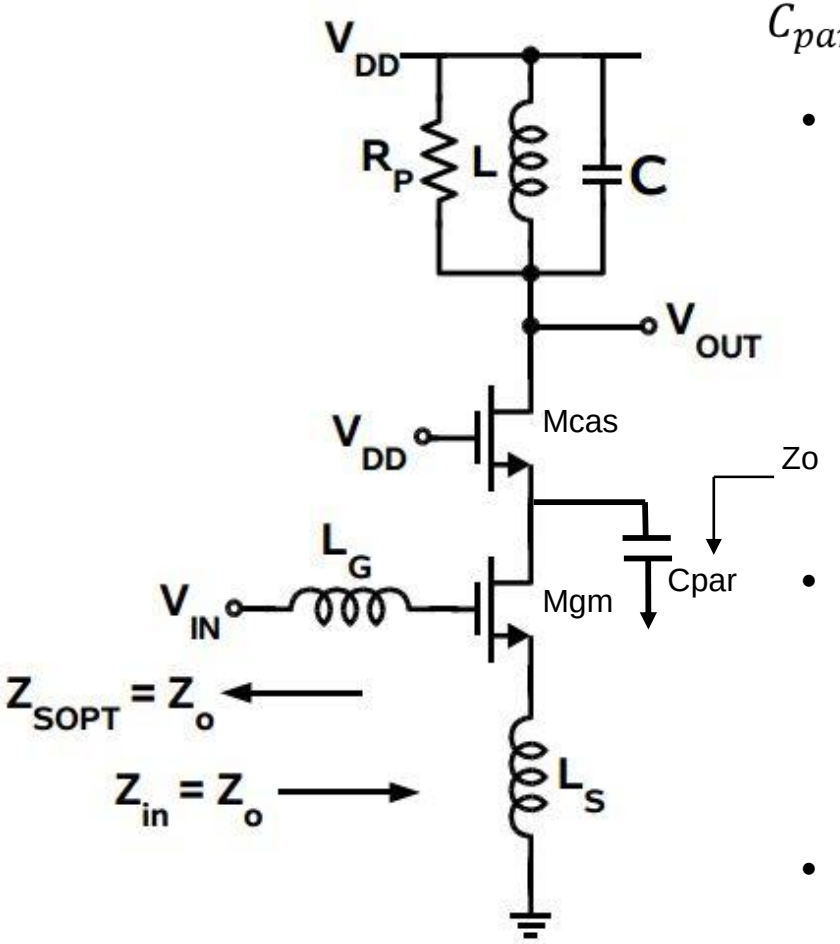
$$i_d = g_m V_{gs\_cas} = -i_{dn} \times \frac{g_m}{g_m + sC_{gs_{cas}}}$$

$$= -i_{dn} \frac{1}{1 - j\frac{\omega}{\omega_T}} \approx -i_{dn}$$

- From equation, cascode device drain noise circulates within the device itself! Therefore it does not reach the output, hence does not degrade NF

What happens if cascode device is too large?

Cascode device size, there is an optimum:



$$C_{par} = C_{d\_Mgm} + \alpha C_{gd\_Mgm} + C_{s\_Mcas} + C_{gs\_Mcas}$$

- As cascode device gets larger, Cpar gets larger as well. This results in reducing Zo, hence a portion of the cascode drain noise current will flow through Zo, hence the derivation of cascode noise we did previously no longer apply and device start to contribute noise.
- Large cascode device also results in gain drop because some of the AC current from Mgm device does not reach Mcas because it flows in Cpar instead.
- Too small of cascode device results in smaller gm of cascode device resulting in larger swing at the Mgm-Mcas interface node, which results in larger distortion

References:

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