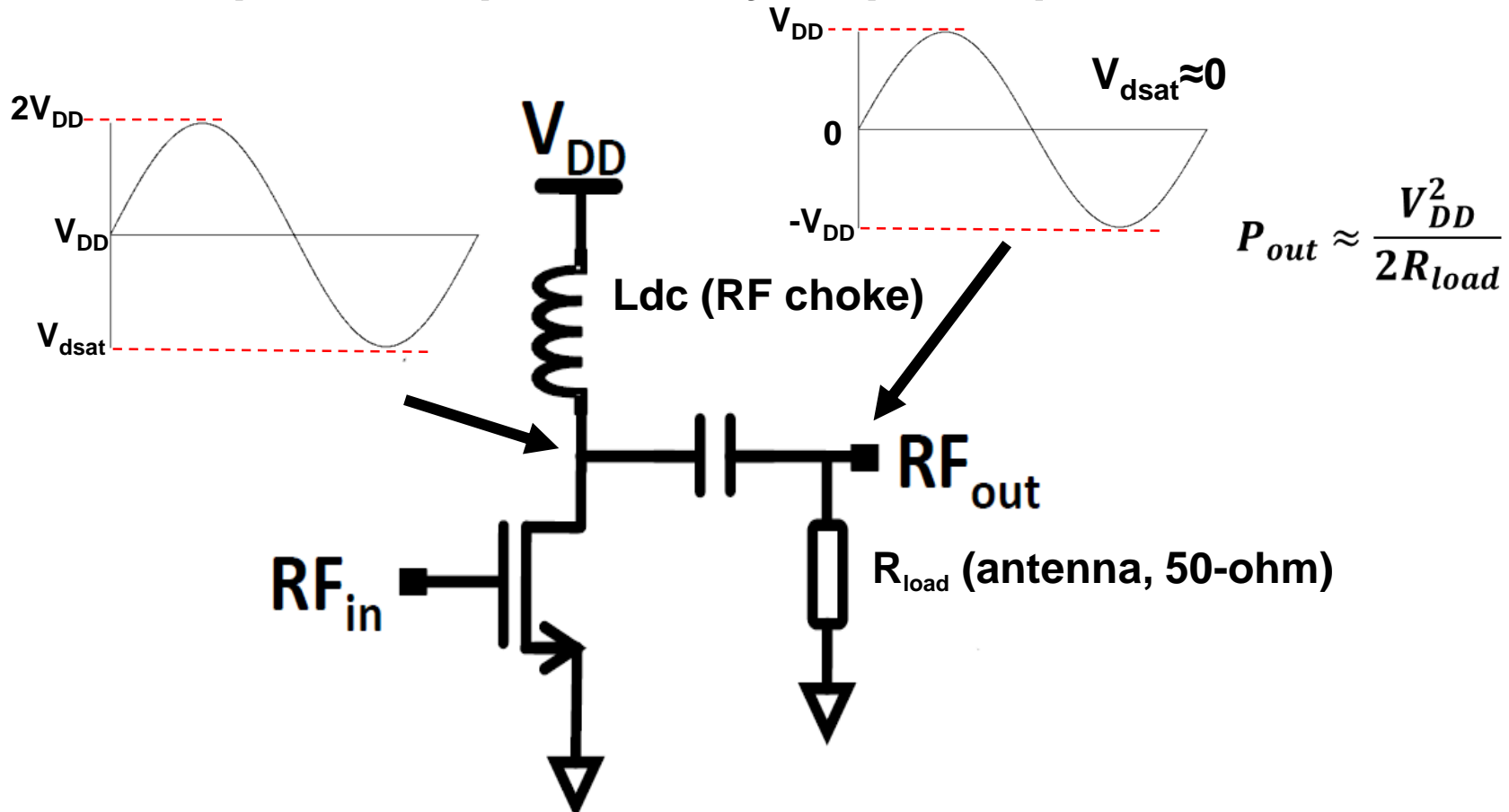# Power Amplifier (PA) design

- **Power Amplifier**
  - function
  - The challenge of delivering high power
  - Load pull
  - Class A, AB, B, C, F, E
 - Memory effects
  - Efficiency enhancement techniques

- **References**

Does a power amplifier really amplifies power?

V_{DD}

$V_{dsat} \approx 0$

$2V_{DD}$

V_{DD}

V_{dsat}

0

$-V_{DD}$

$$P_{out} \approx \frac{V_{DD}^2}{2R_{load}}$$

V_{DD}

Ldc (RF choke)

RF$_{out}$

RF$_{in}$

R$_{load}$ (antenna, 50-ohm)

● a power amplifiers converts DC power (from power supply) to RF power (as efficiently as possible). This is kind of different from "small-signal" blocks such as an LNA

The challenge of delivering high-power in CMOS:
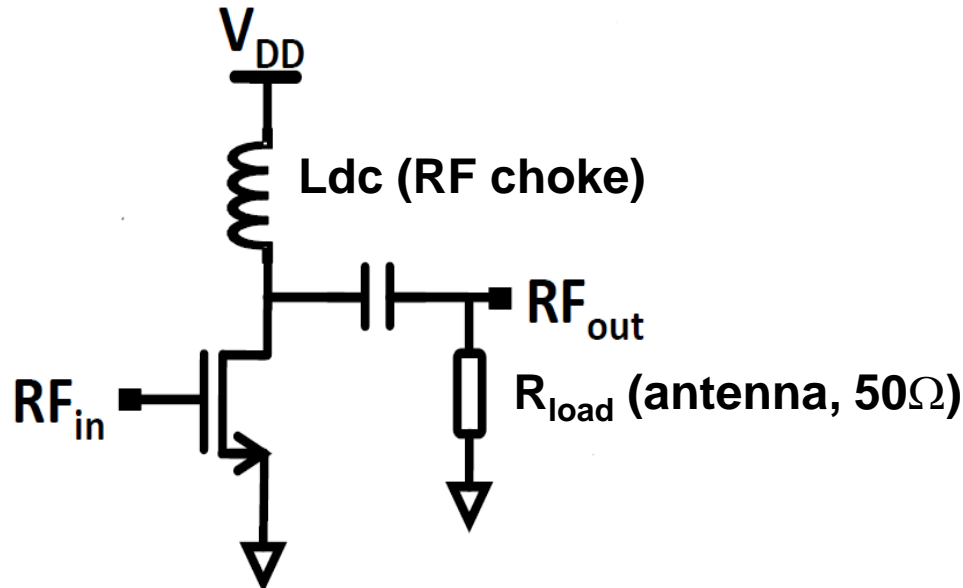
$$P_{out} \approx \frac{V_{DD}^2}{2R_{load}}$$

- from the above equation, to deliver +30dBm (1Watt) output power to the 50Ω load, V_{DD} needs to be 10V !!

- If CMOS technology of say 55nm is used with HCI reliability limit of 1.3V only, the device will breakdown and so cannot deliver this power. The max power that can reliably be delivered to such a load is $(1.3)^2/100 = 17$mW (~12dBm)!

→ What to do?

Reliability of CMOS device and stress mechanisms: HCI
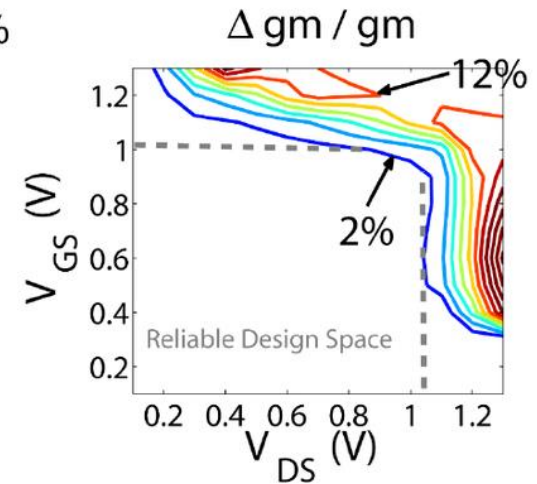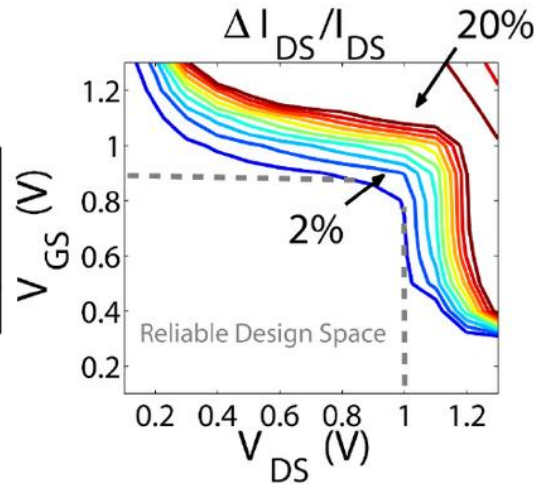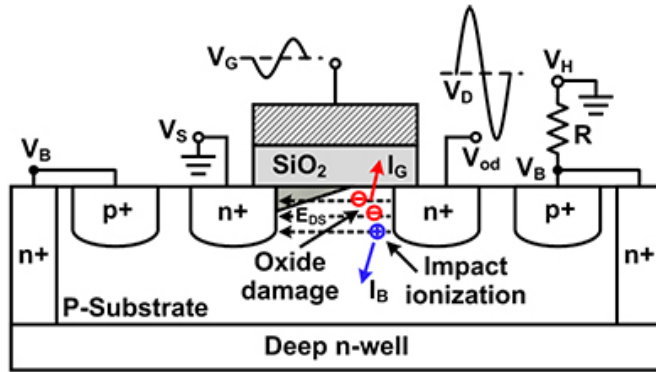
- Hot Carrier Injection (HCI) happens when device is ON (channel is inverted) and there is large horizontal electric field present due to large Vds.

- Electron carriers experience large velocity and get injected into the oxide shifting the device threshold voltage over time (it is a life time degradation issue)

- Issue is alleviated by reducing Vds/Vgs and/or increase device channel length

Reliability of CMOS device and stress mechanisms: NCS
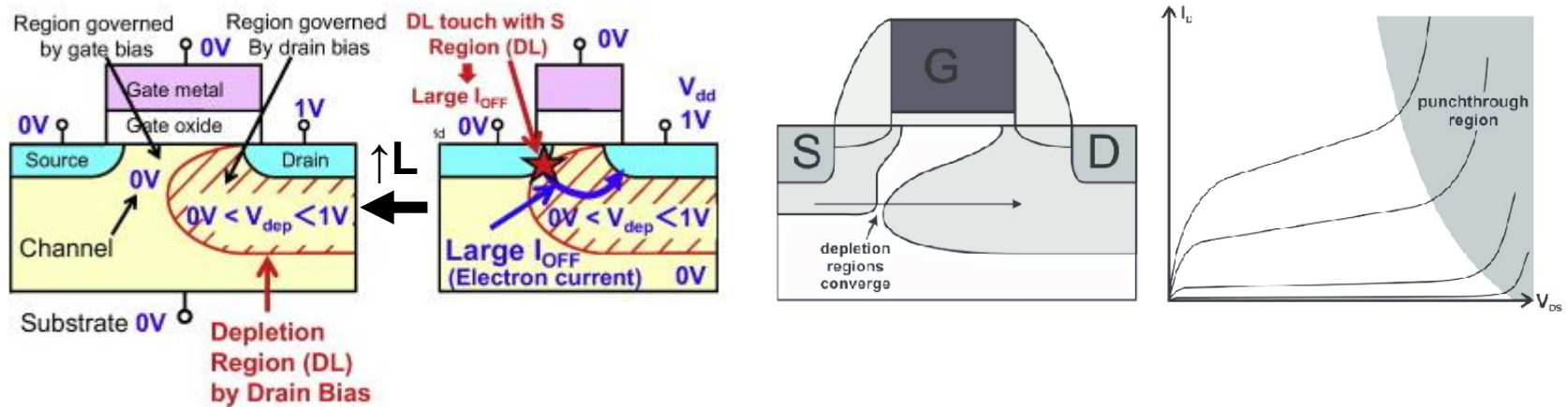
- None-Conductive Stress, also known as Punch Through, happens when the device is not conducting any current (off) while there is a large Vds voltage across the device

- Depletion region of drain extends towards source increasing leakage current, hence device off-region Rds.

- Issue is alleviated by reducing Vds and/or increase device channel length

- NCS voltage rating is usually much higher than its HCI for a given technology

- NCS is not destructive unless large currents causes thermal or electron-migration damage

# Reliability of CMOS device and stress mechanisms: Oxide BD
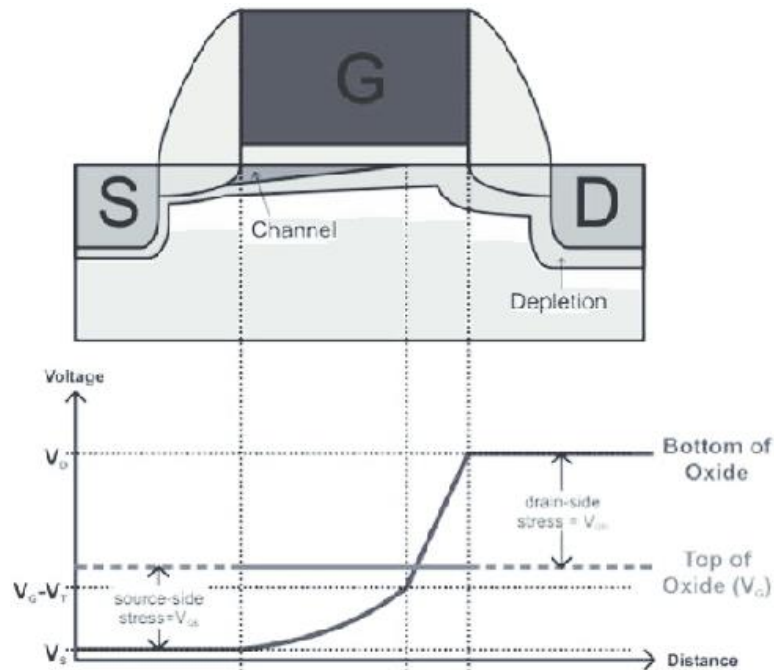
- Oxide breakdown (BD) happens when large Vgs or Vdg exceed the rating

- Oxide breakdown is a catastrophic damage (instant, cannot recover)

- There is usually no difference between AC and DC signals (the moment the voltage crosses the breakdown threshold, damage occurs)

- Oxide BD can only be alleviated by lowering voltage (or of course use thicker oxide device)

# Reliability of CMOS device and stress mechanisms: TDDB
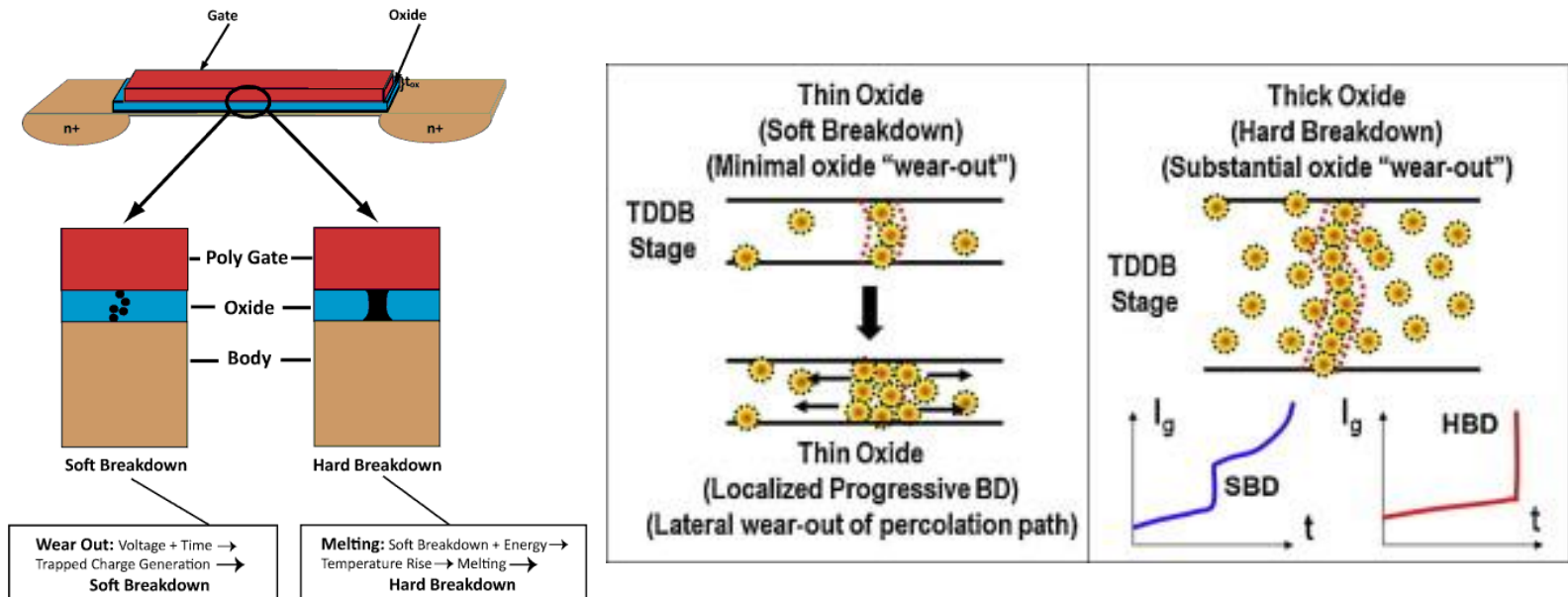
- Time-Dependent Dielectric Breakdown (TDDB) is a "wear-out" mechanism of the device oxide due to defects that degrades (or destroys) device over time.

- It is a statistical process (two devices with same terminal voltages may fail at different times)

- Defects in the oxide can be due to manufacturing or due to gate tunneling effect in thin-oxide

- TDDB rating is inversely proportional to device oxide area. It can only be alleviated by lowering voltage (or of course use thicker oxide device)

# Important issues about device reliability metrics: HCI, TDDB, NCS, ..
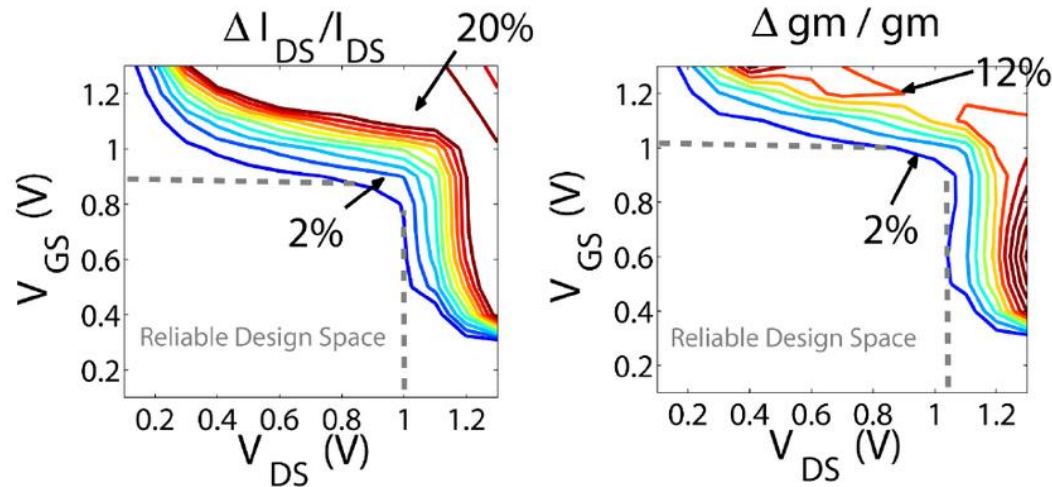
- The pass/fail voltage rating is done at the device level (for example when Vth shifts by 10mV or when Idss changes by 10%). These numbers have nothing to do with PA performance (in many cases PA is just fine if Vth shifts by 10mV)

- In some of these reliability mechanisms, there is a difference between AC and DC signals (device can tolerate larger AC swing than constant DC voltage). The AC signal nature (CW, OFDM, etc,) also another factor (device can tolerate OFDM signal more than CW tone with same peak value).

- PA design is all about pushing these limits and design a circuit that is reliable for the target application but not being very conservative (foundry gives very conservative device reliability numbers usually related to DC voltages)

→ Understanding device reliability and its impact on PA performance is KEY. PA burn-in in the lab is best way to design PAs while pushing these limits

SEM photos of actual PA failures:

CONT layer
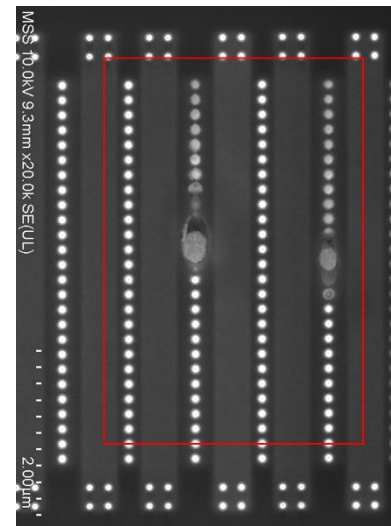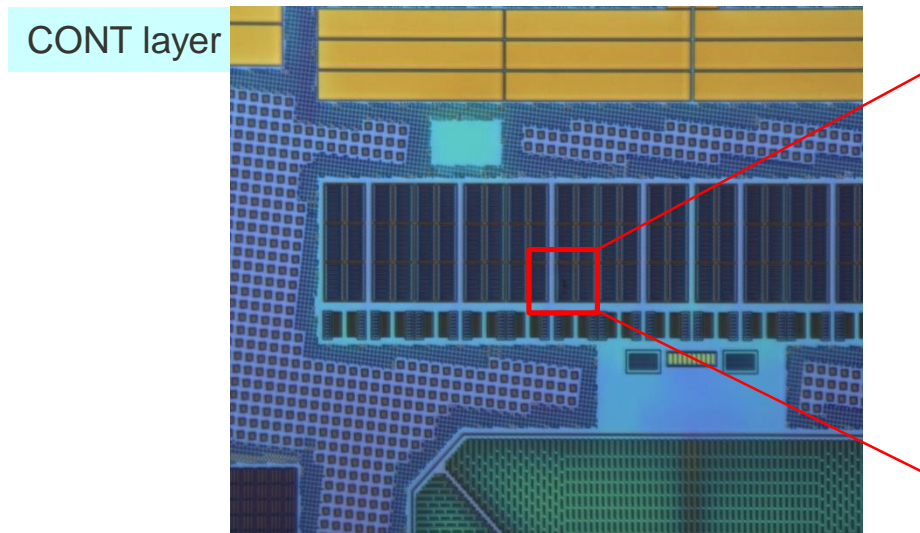
Oxide BD(large gate leakage current, likely TDDB)
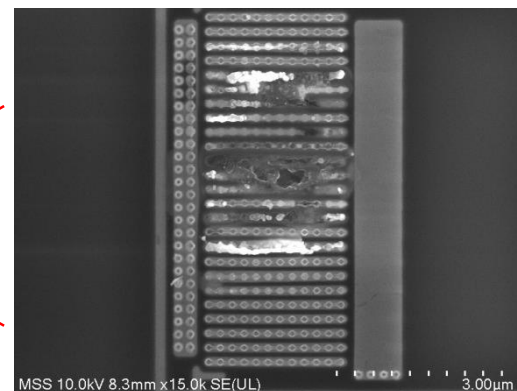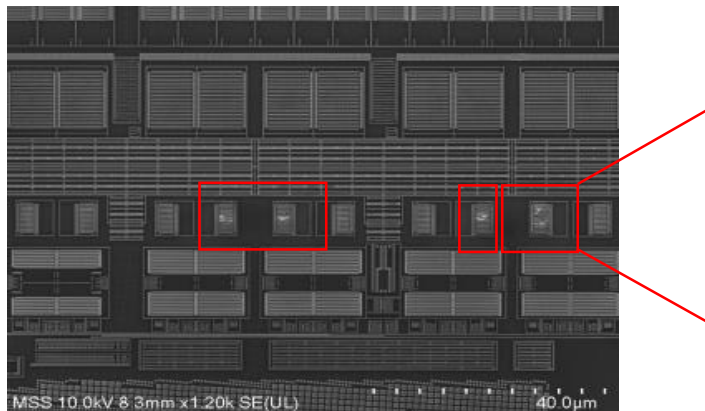
NCS failure resulting in high current damage on D/S metal (EM)

- Failure analysis (FA) can lead you to which device fails and which port (gate, drain) has the damage for you to analyze the failure mechanism and adjust PA design to fix the issue

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The challenge of delivering high-power in CMOS:
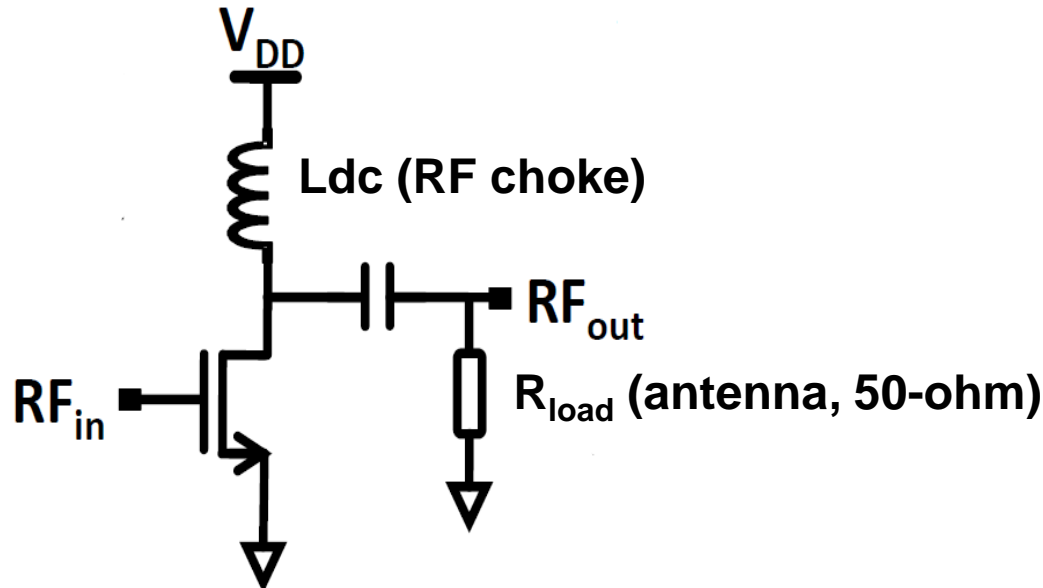
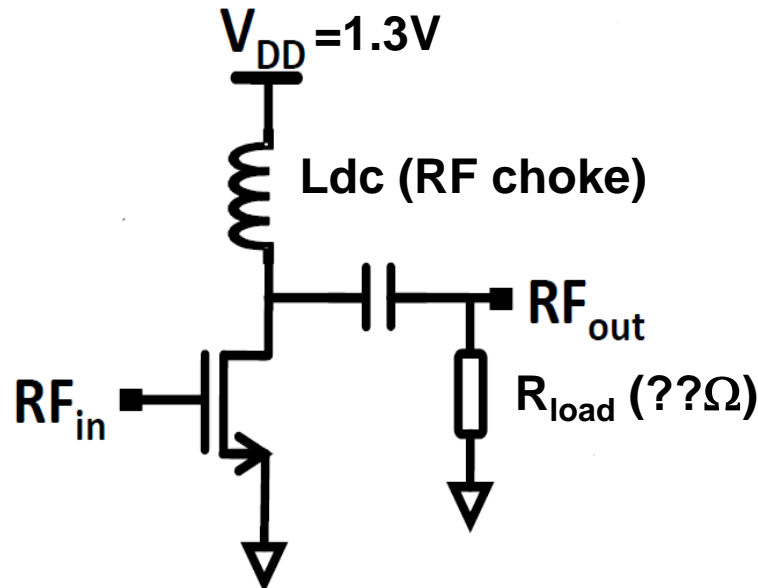$$P_{out} \approx \frac{V_{DD}^2}{2R_{load}}$$

- from the above equation, to deliver 30dBm (1Watt) output power to the 50-ohm load, V_{DD} needs to be 10V !!

- If CMOS technology of say 55nm is used with HCI reliability limit of 1.3V only, the device will breakdown and so cannot deliver this power. The max power that can reliably be delivered to such a load is $(1.3)^2/100 = 17mW$ (~12dBm)!

→ What to do?

R_load of PA to deliver high Pout:

$$P_{out} \approx \frac{V_{DD}^2}{2R_{load}}$$

$$\rightarrow R_{load} \approx \frac{V_{DD}^2}{2P_{out}}$$

- With V_{DD} is set to **1.3V** to match the max reliability V_{ds} of thin-gate 55nm device, we can then calculate Rload needed to deliver **30dBm** power:

→ R_{load} = **0.85Ω**! This is very small load resistor to be realized practically with on-chip components (need to still match to the 50Ω antenna)
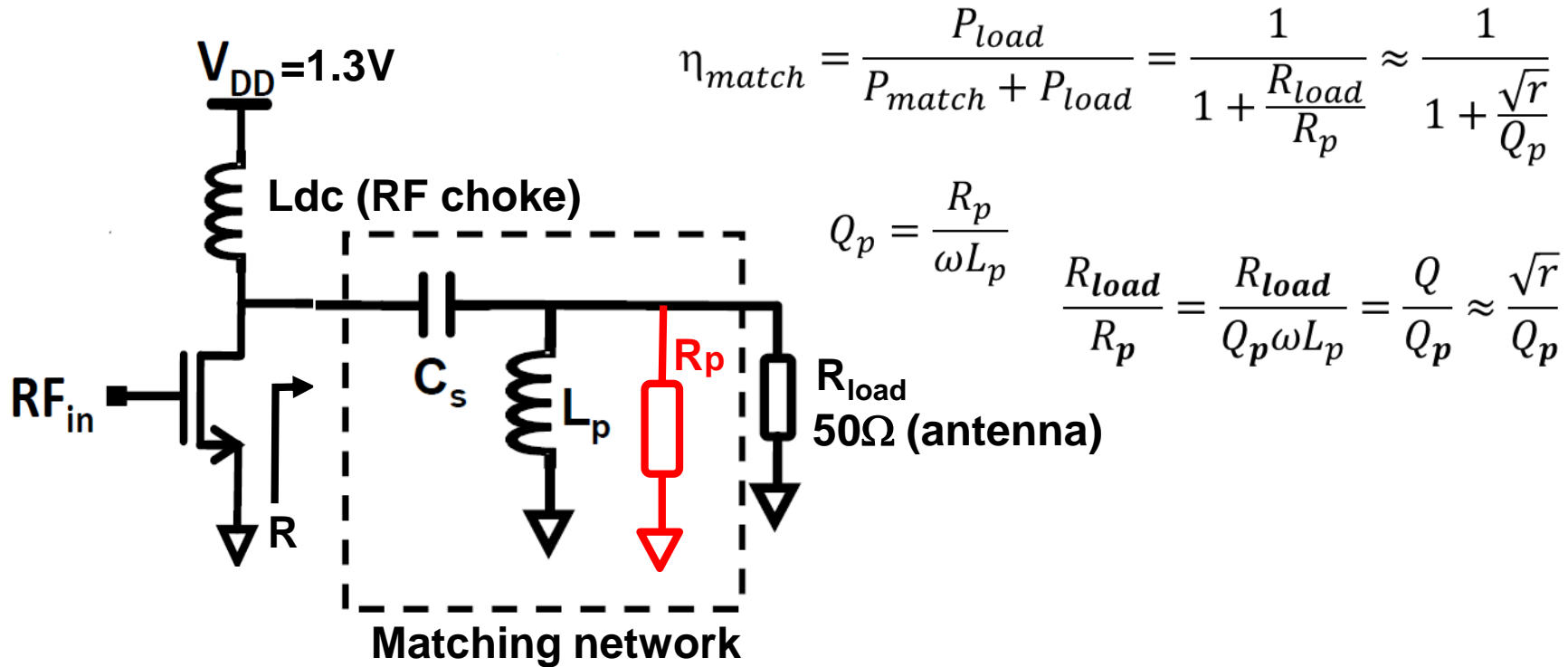
Let us find out why

Matching PA load to 50Ω:
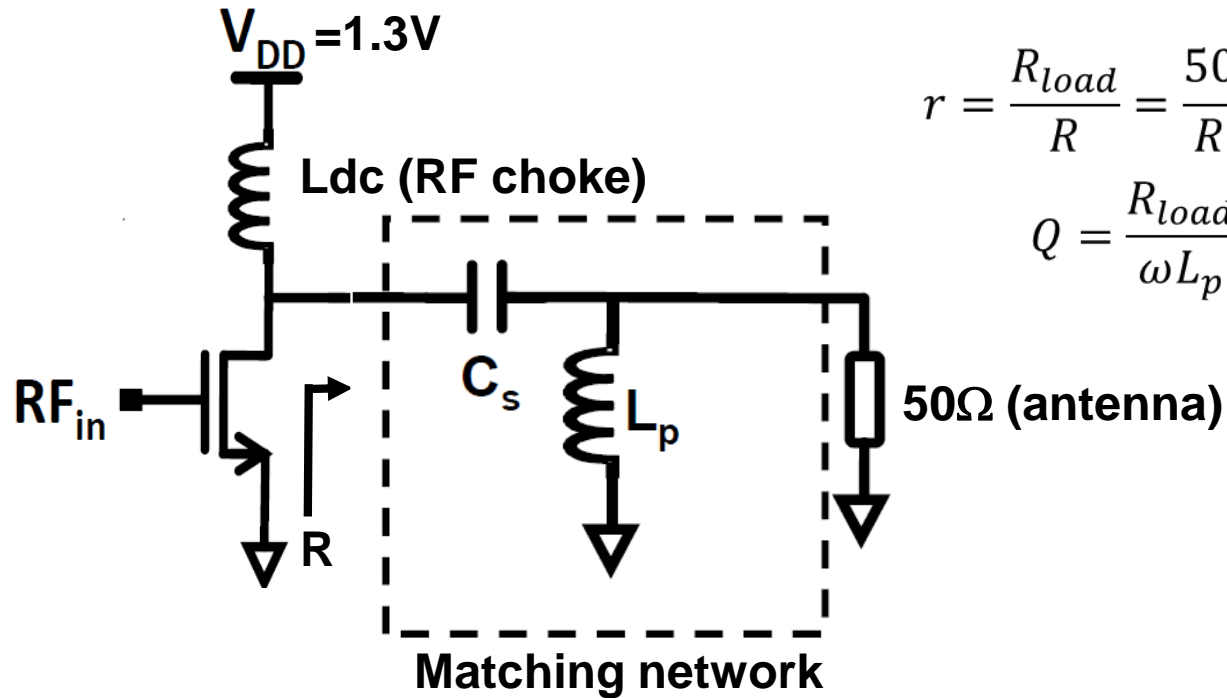
$$r = \frac{R_{load}}{R} = \frac{50}{R} = 1 + Q^2$$

$$Q = \frac{R_{load}}{\omega L_p}$$

- In our example, with R=0.85Ω, the network Q is ~7.6.

→ This may not sound too bad. However, the issue is the finite Q of on-chip matching network as explained next

Finite Q of on-chip matching passives:

$$\eta_{match} = \frac{P_{load}}{P_{match} + P_{load}} = \frac{1}{1 + \frac{R_{load}}{R_p}} \approx \frac{1}{1 + \frac{\sqrt{r}}{Q_p}}$$

$$Q_p = \frac{R_p}{\omega L_p}$$

$$\frac{R_{load}}{R_p} = \frac{R_{load}}{Q_p \omega L_p} = \frac{Q}{Q_p} \approx \frac{\sqrt{r}}{Q_p}$$

Matching network

- The finite Q of matching network results in efficiency degradation of matching network (power loss)

→ For say 80% matching network efficiency (η_{match}), in our example (R = 0.85Ω) Qp needs to be around ~31. This is hard to realize with on-chip inductors

Impact of finite Q of on-chip matching components:
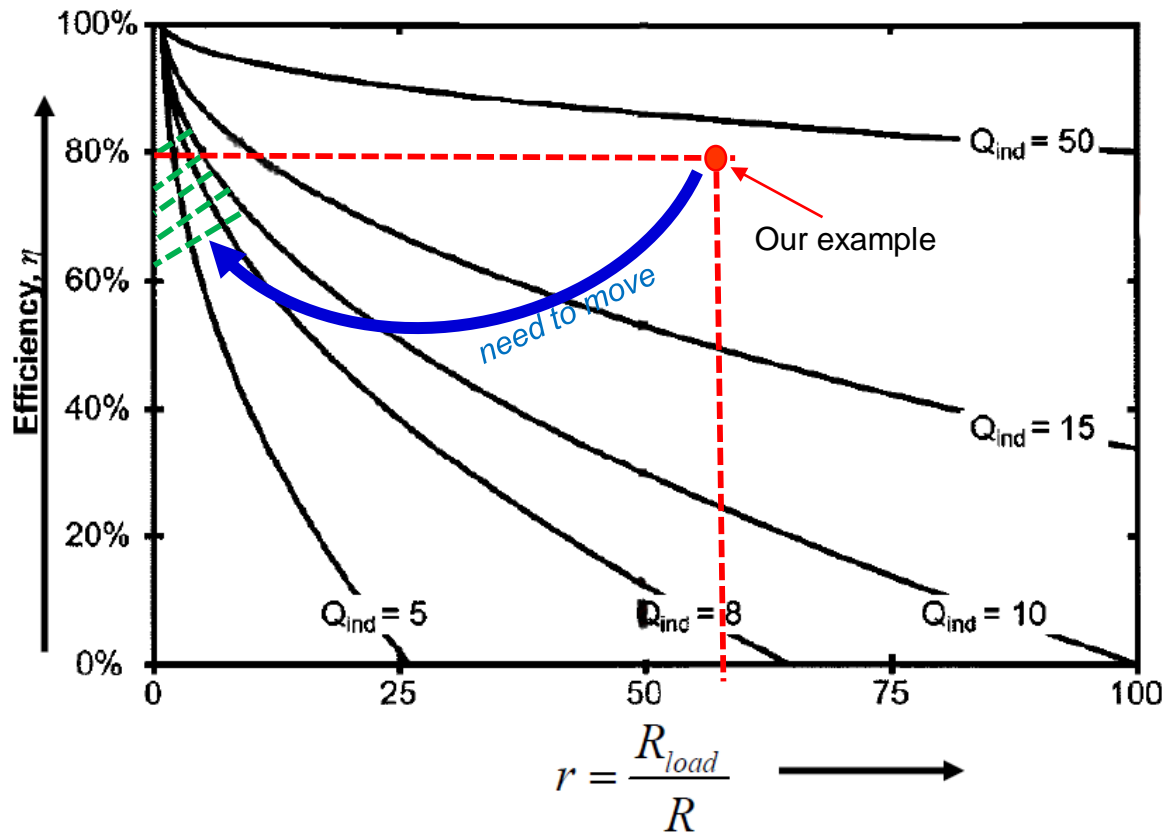
- Need to operate within the region of realizable on-chip inductors Q (<13)

→ For matching network efficiency η>70%, the only way to do this with on-chip matching is by reducing ↓*r*, which means increasing ↑*R*. This means for same output power we need to increase ↑**swing** without violating reliability limits!

→ How?

# Increase swing without affecting reliability: use differential circuit
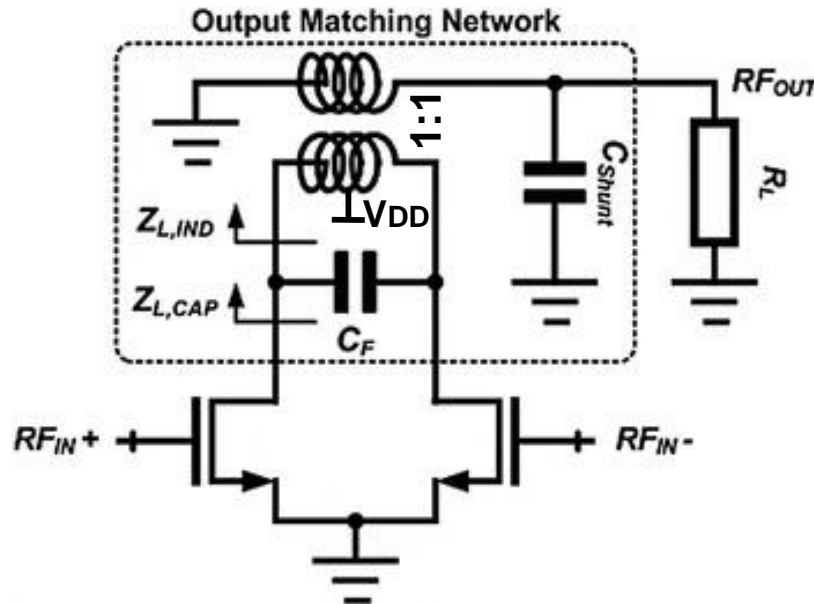
$$P_{out} \approx \frac{2V_{DD}^2}{R_{load}}$$

$$\rightarrow R_{load} \approx \frac{2V_{DD}^2}{P_{out}}$$

- For same V_{DD} and target P_{out} as before, the differential **R** can now be 4x larger or in our example is 4 x 0.85 = 3.4Ω. This brings **r** down to ~15.

- Although this is better than before and matching can be realized by on-chip components, however, the loss is quite large and efficiency is <70% for inductor Q of 8 or 10

→ Still need to reduce **r** further. The only thing left is to increase V_{DD} without affecting reliability.

How?

## Increase V_{DD} using thick-gate cascode device:
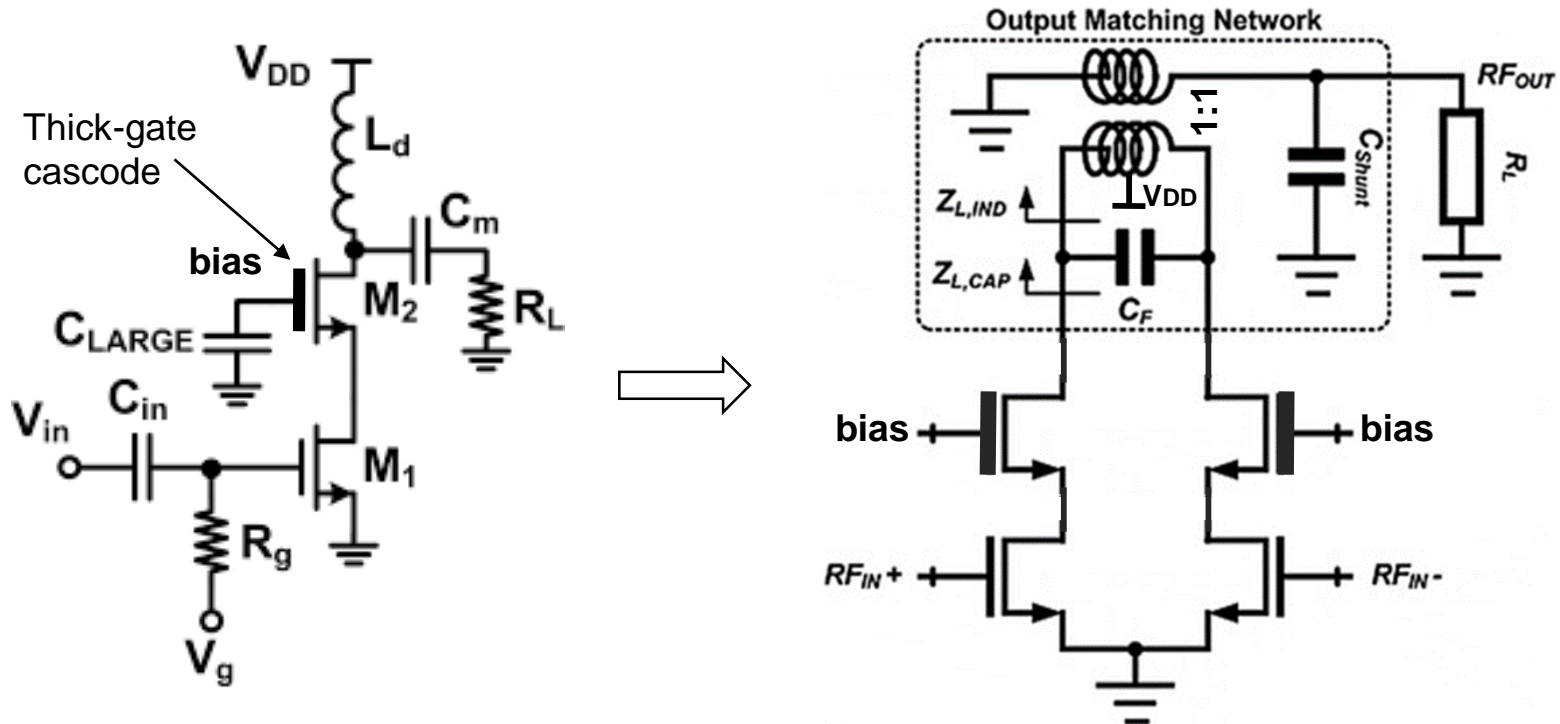
- A thick-gate cascode device can be used to be able to increase V_{DD}. The cascode device can handle the large output swing while protecting the bottom CS thin-gate device which provides the PA gm and gain.

→ Using an I/O device (thick-gate, L=0.28μm) in 55nm, V_{DD} can be increased to 3.3V. For the differential topology and for same Pout, this brings **R** to ~22Ω. This in turn brings **r** to ~2.3. Now matching network can comfortably be realized with on-chip inductors of Q=8 and efficiency is close to 90%.

# Increase V_{DD} using "special" High-voltage cascode device:

DEMOS
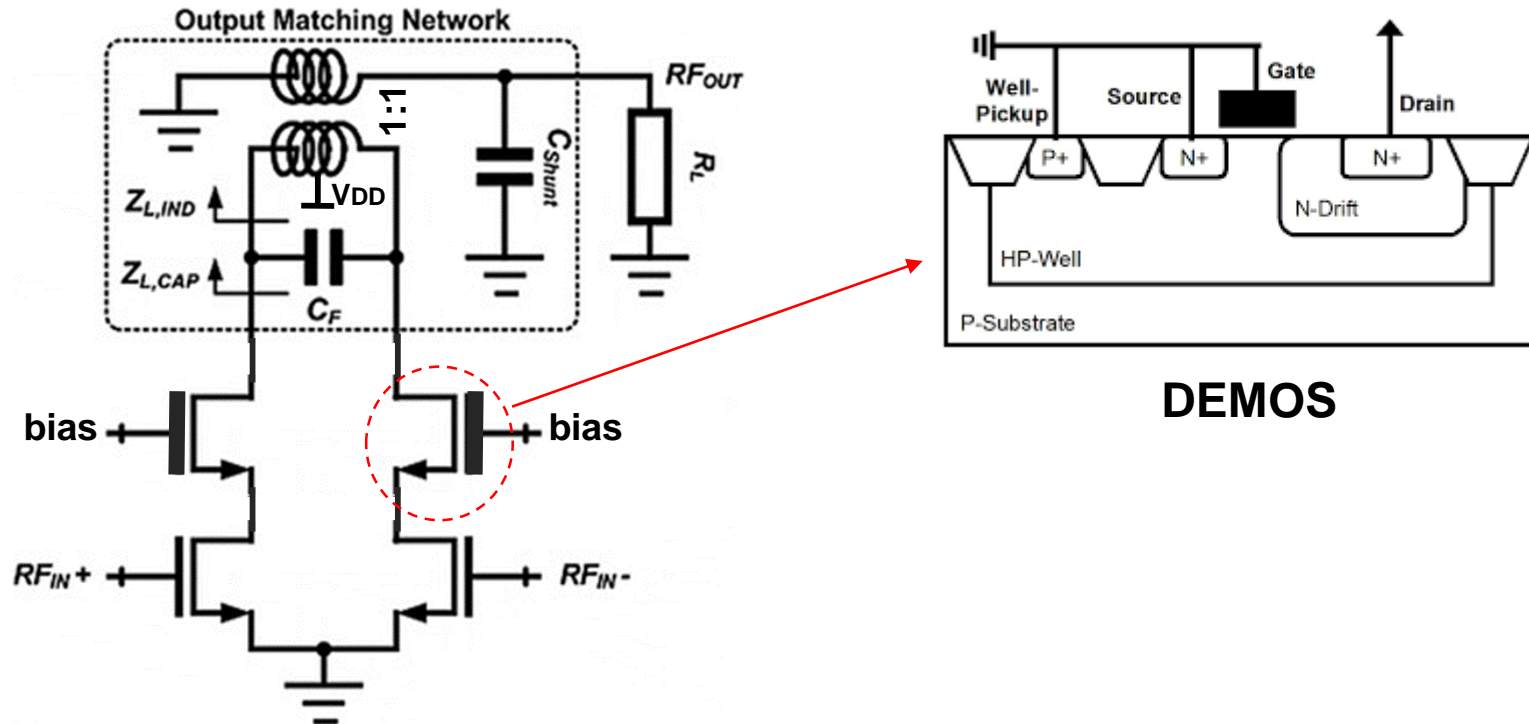
- Drain-extension using lightly doped n-well region increases punch-through Vds voltage to 7~10V. The gate-oxide also does not overlap with the drain n+ region improving Vgd oxide breakdown voltage.

- The device usually comes for "free!" with no extra mask is needed

- The f_T of such device is decent (25~35GHz in 55nm technology). Drain parasitic cap is large and can impact PA distortion (AM-PM)

- "knee voltage" of the device maybe a bit larger than normal I/O device

Limitation of PA V_{DD}:

Supply

PMU

PA

Li-Ion 2.7~4.2V

DC-DC

V_{DD}

PCIe 3.3V

LDO

PA

Wire!

USB 5V
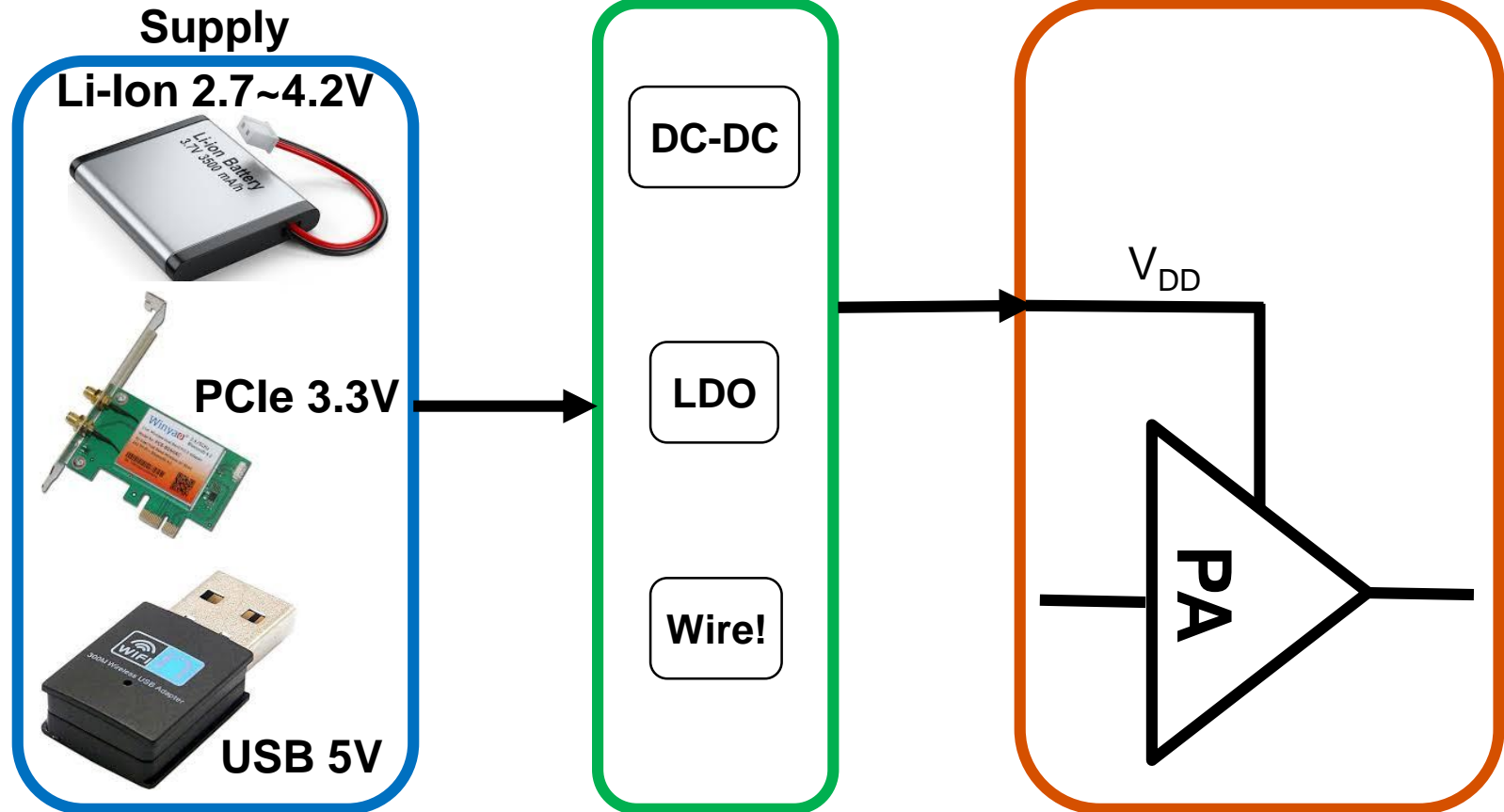
- V_{DD} value in many cases is not a design option. It is usually set by the application. To make V_{DD} a design parameter you need to build a buck-boost DC-DC converter only for the PA, which may not be cost effective in some applications. A cheaper way is to build an LDO but this is not good for efficiency. In ultra-low cost application, the PA needs to interface directly with the supply

Matching using balun:
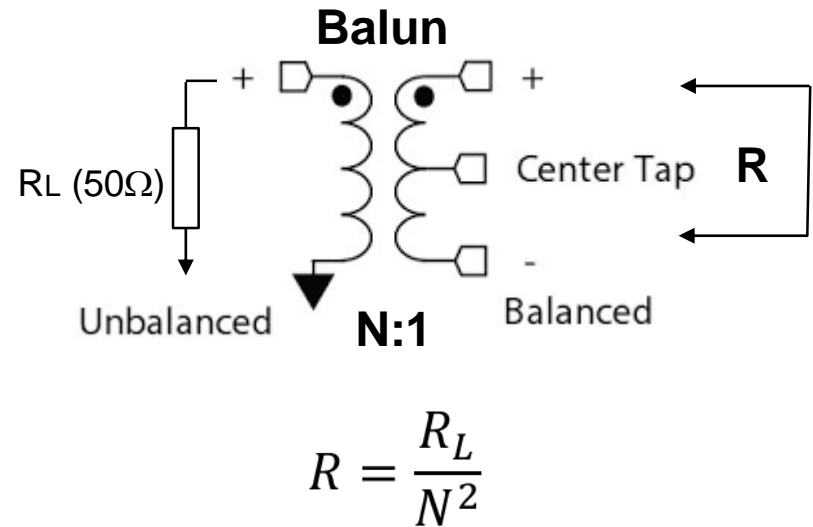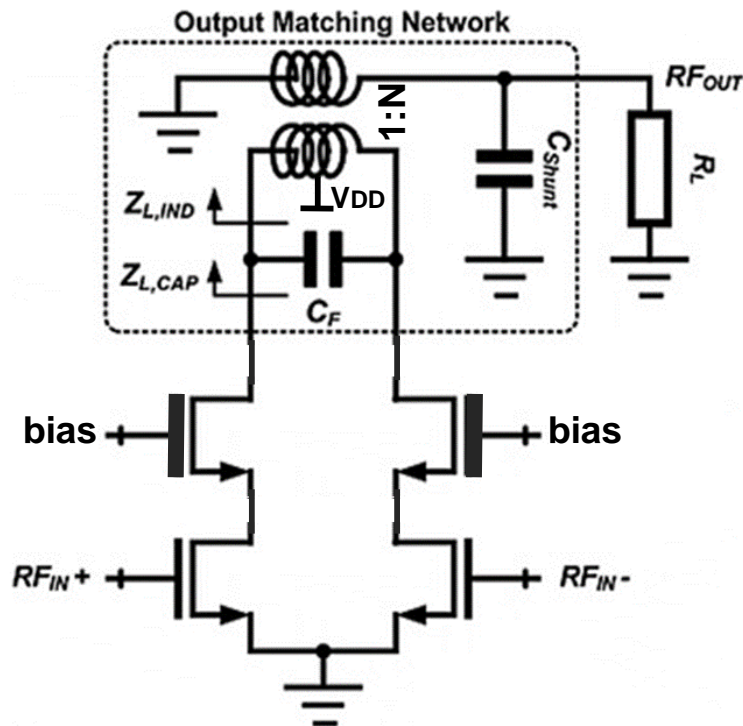
- For a given **R** the PA likes to see, balun N can be calculated for output matching. For example, if R=12Ω, a 1:2 balun can be used to match this PA impedance to 50Ω.

- Large N results in lower balun Q (multi-turns) which increases balun loss and so reduces PA efficiency

Few considerations:

Output Matching Network

"knee"

"knee voltage"
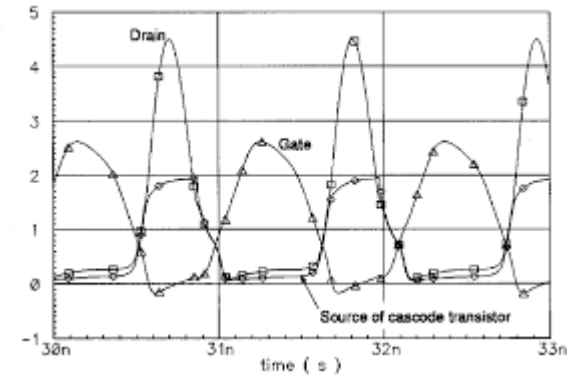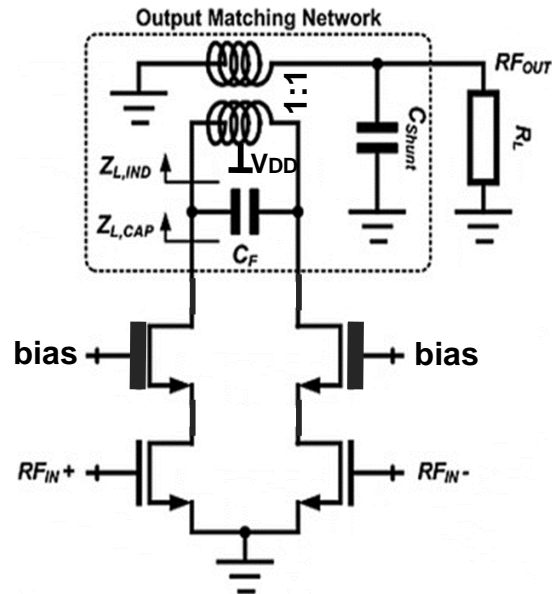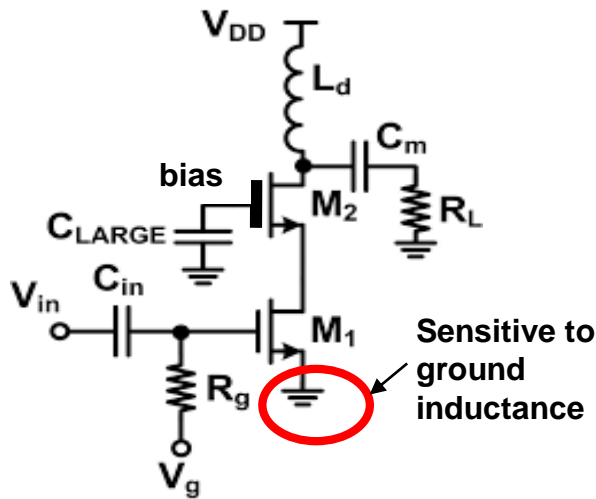
- Single-ended PA is quite sensitive to ground inductance. Low ground inductance are hard to realize on-chip with finite package inductance. The inductance impacts PA gain and power added efficiency. Differential PA does not have this issue.

- Adding a cascode device increases the "knee voltage" of the PA. Using HV-MOS increases the knee voltage even further. This impacts PA swing, Pout and efficiency
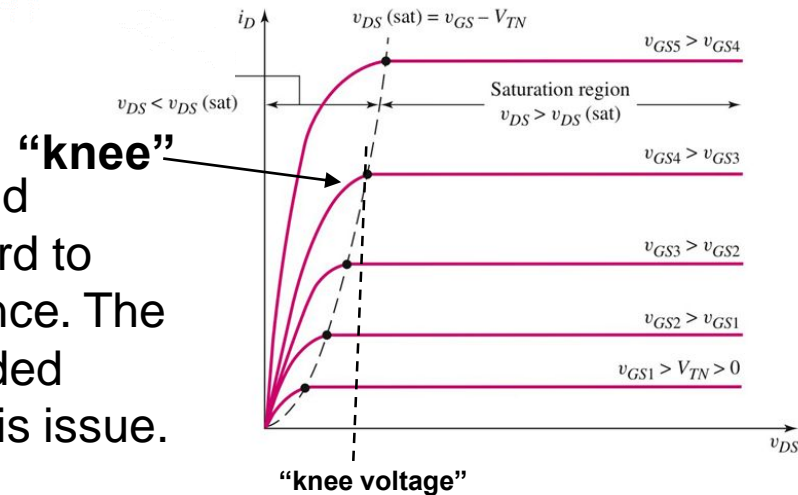
What if there is no HVMOS device in a process? power combining:
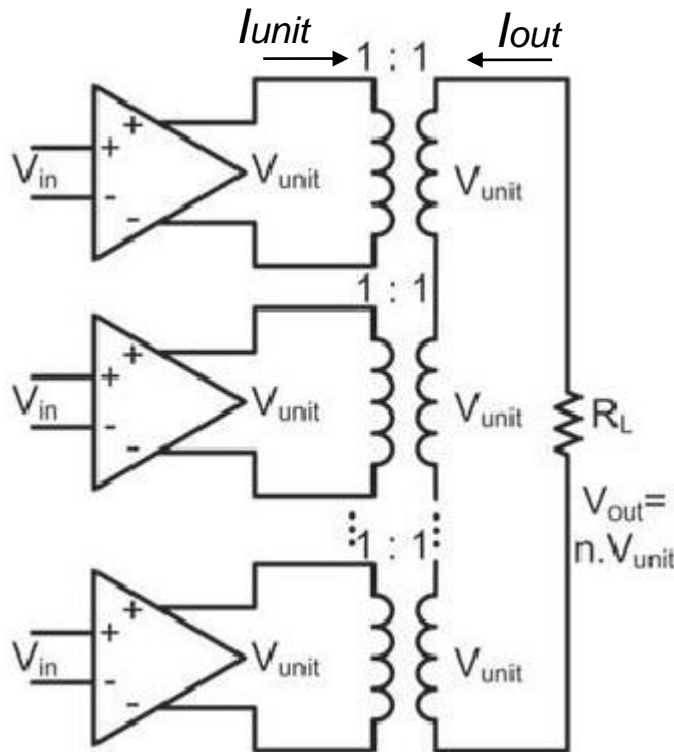
$$V_{out} = nV_{unit}$$
$$I_{out} = I_{unit}$$
$$\rightarrow P_{out} = nP_{unit}$$

- In the case where there is no high-voltage device to be used in a cascode (for example in FinFet process), power combining is perhaps your best choice for PA architecture

- Power combining uses smaller PAs (each delivering relatively small power within its reliability capability) and combine them using passive combiner

- As the number of PAs increases, the power combiner design gets complicated and its loss increases. Therefore, there is an optimum number of PAs in a given process.

Important metrics for PA:

$$P_{DC} = V_{DD}I_{DD}$$
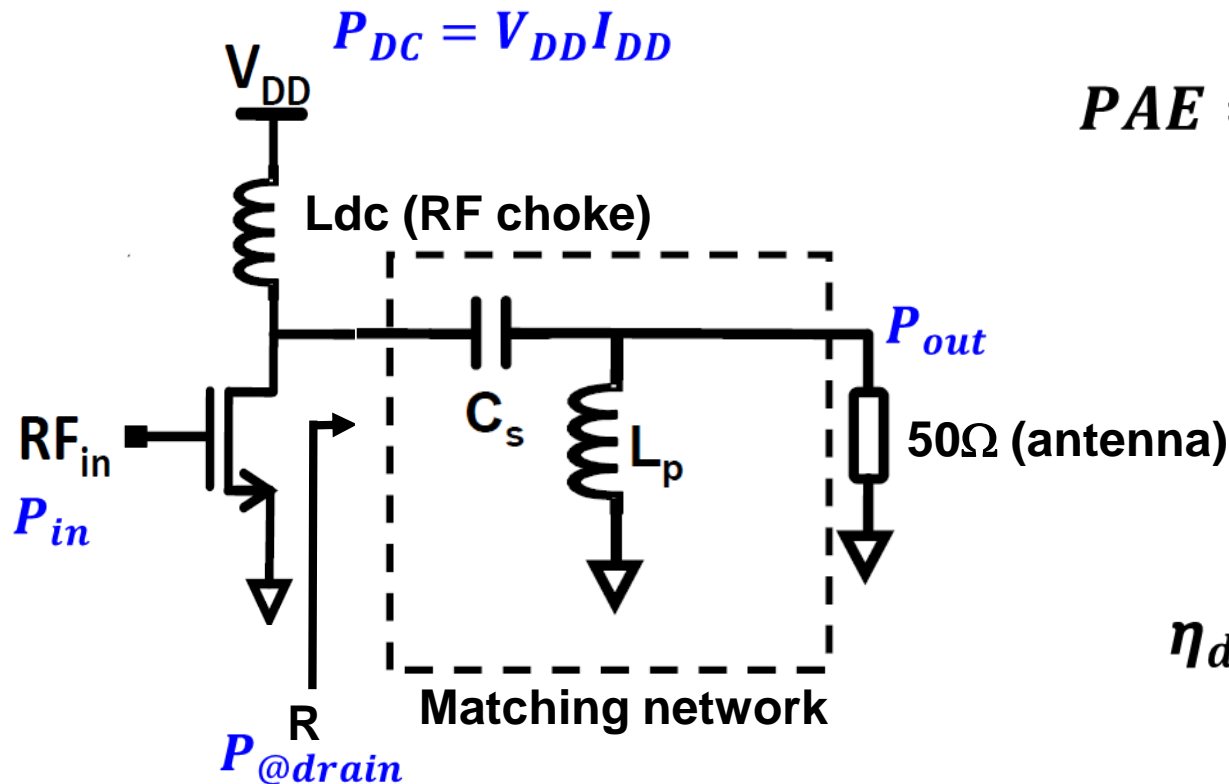
$$PAE = \frac{P_{out} - P_{in}}{P_{DC}}$$

$$\eta_{load} = \frac{P_{out}}{P_{DC}}$$

$$\eta_{drain} = \frac{P_{@drain}}{P_{DC}}$$

V$_{DD}$

Ldc (RF choke)

P_{out}

RF$_{in}$

P_{in}

C$_s$

L$_p$

50Ω (antenna)

R

$P_{@drain}$

Matching network

- Drain efficiency, η_{drain}, is the efficiency at the drain of the PA by calculating the power delivered by the drain node of the PA relative to DC power from supply. It does not include any matching network losses. This metric tells you how good your PA core is

PA distortion: Static AM-AM and AM-PM
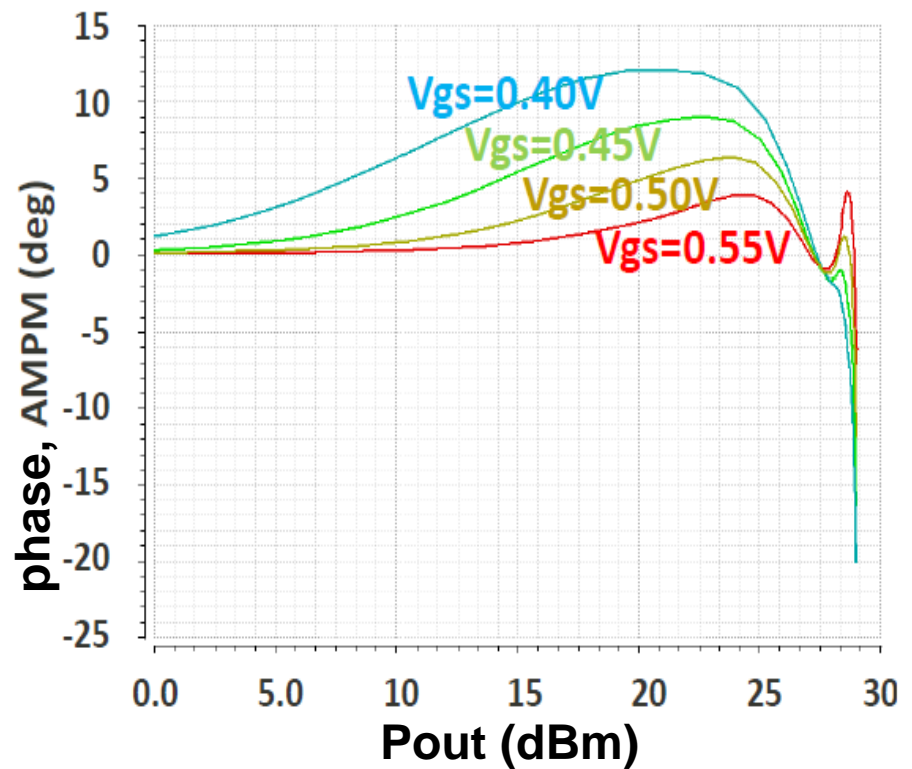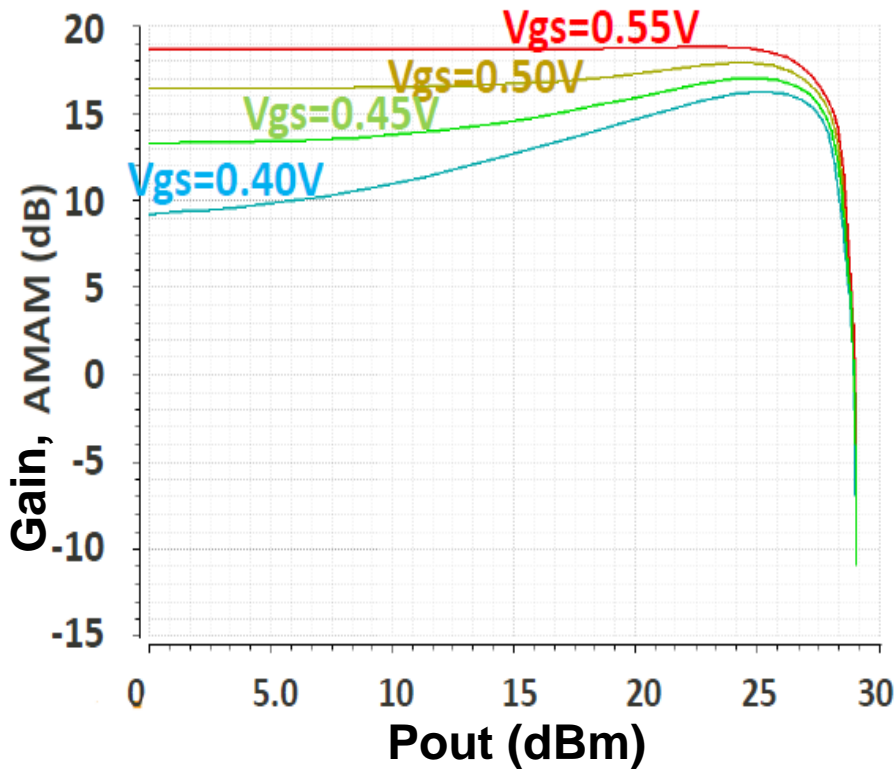
- AM-AM distortion is mainly due to 3rd order distortion of the PA, as discussed in a previous lecture (and sometimes higher odd order distortion like 5th) . AM-PM distortion is due to non-linear capacitors in the PA circuit

- Plots are generated by sweeping input CW tone amplitude and record gain and phase of output vs Pout

PA distortion: dynamic, memory effects
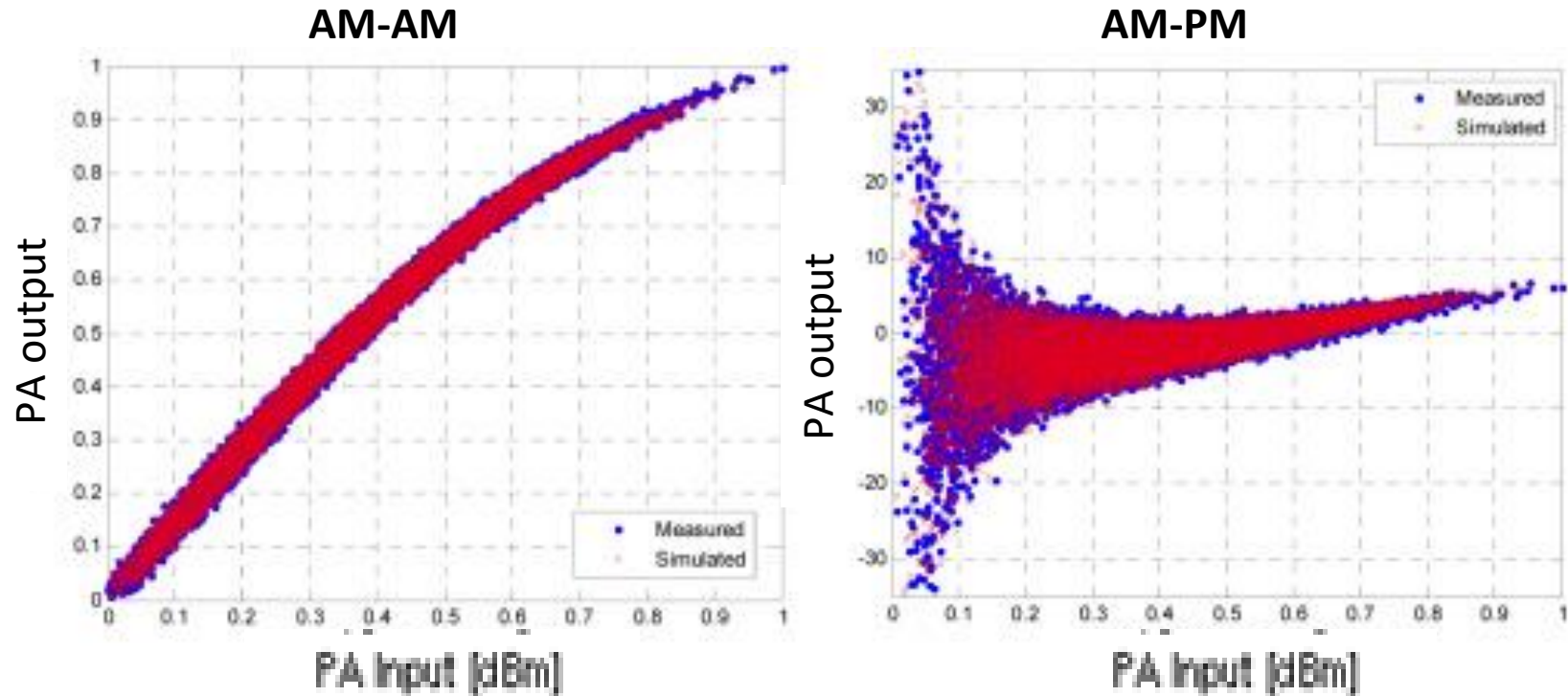
AM-AM　　　　　　　　　　　　　　　**AM-PM**

- memory effect is when the PA output, at a given time, depends also on the instantaneous input that happened earlier
- problem gets worse with wider signal bandwidth
- the "thicker" the AM-AM/PM traces are the worse are memory effects

PA distortion: dynamic, memory effects' signature

ω_1 ω_2

IM3$_h$

Δ IM3$_L$

Freq (Hz)
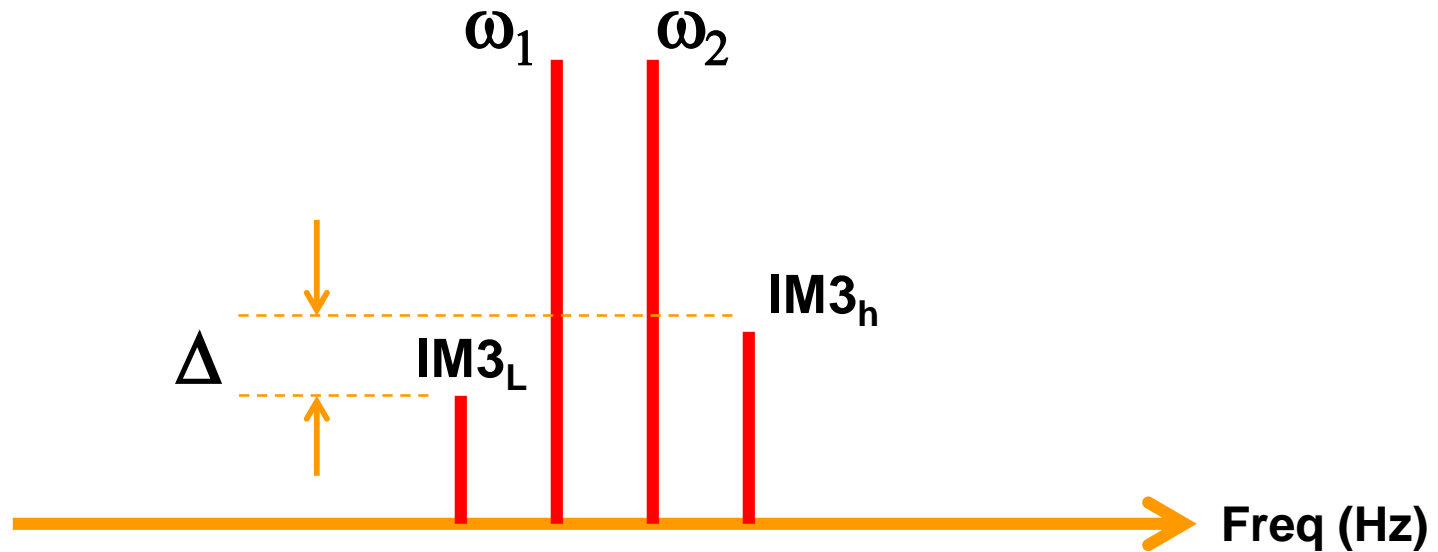
• it is not the asymmetric IM3, but that the asymmetry <u>changes</u> as a function of tone pacing (signal bandwidth)

PA distortion: memory effects, cause
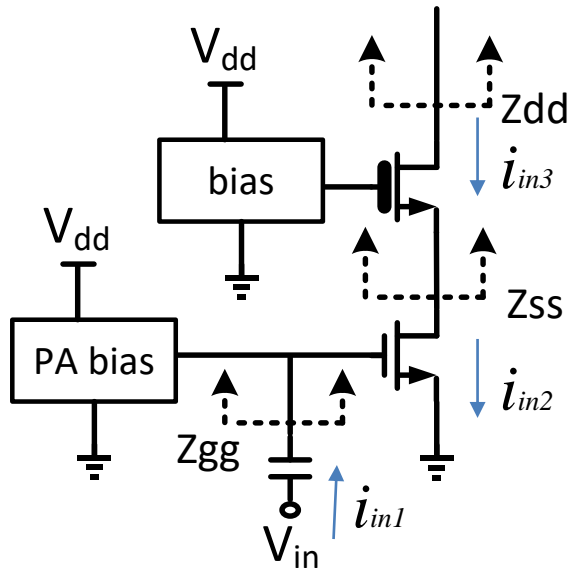
$$i_{in}(t) = m(t)\cos(\omega_0 t + \varphi(t))$$

at any node of the PA there exists nonelinear ity

$$v_{node}(t) = Z_1 i_{in}(t) + Z_2 i_{in}^2(t) + Z_3 i_{in}^3(t) + ...$$

$$= ... + Z_2\left[m^2(t) + m^2(t)\cos(2\omega_0 t + 2\varphi(t)) \right] + ...$$

Envelop   *HD2*

- memory effects are caused by the impedance at any node of the PA being frequency dependent (not purely resistive, has a time constant or delay) over the signal envelop bandwidth (tone spacing baseband frequency)
- Similar behavior if impedance phase changes over HD2
- results in un-balanced upper and lower IM3 and becomes tone spacing (bandwidth) dependent
- Need to address both the source of memory effects and the transfer function by which memory effects gets inband

Memory effects: IM3 asymmetry due to RF HD2

$\equiv$ PA nonlinearity

ω_1 ω_2

$2\omega_2 - \omega_1$

$IM3_h$

$2\omega_1$ $2\omega_2$

$2\omega_1 - \omega_2$

$IM3_L$

- IM3 due to HD2 adds on top of PA IM3 either constructively or destructively, depending on phase
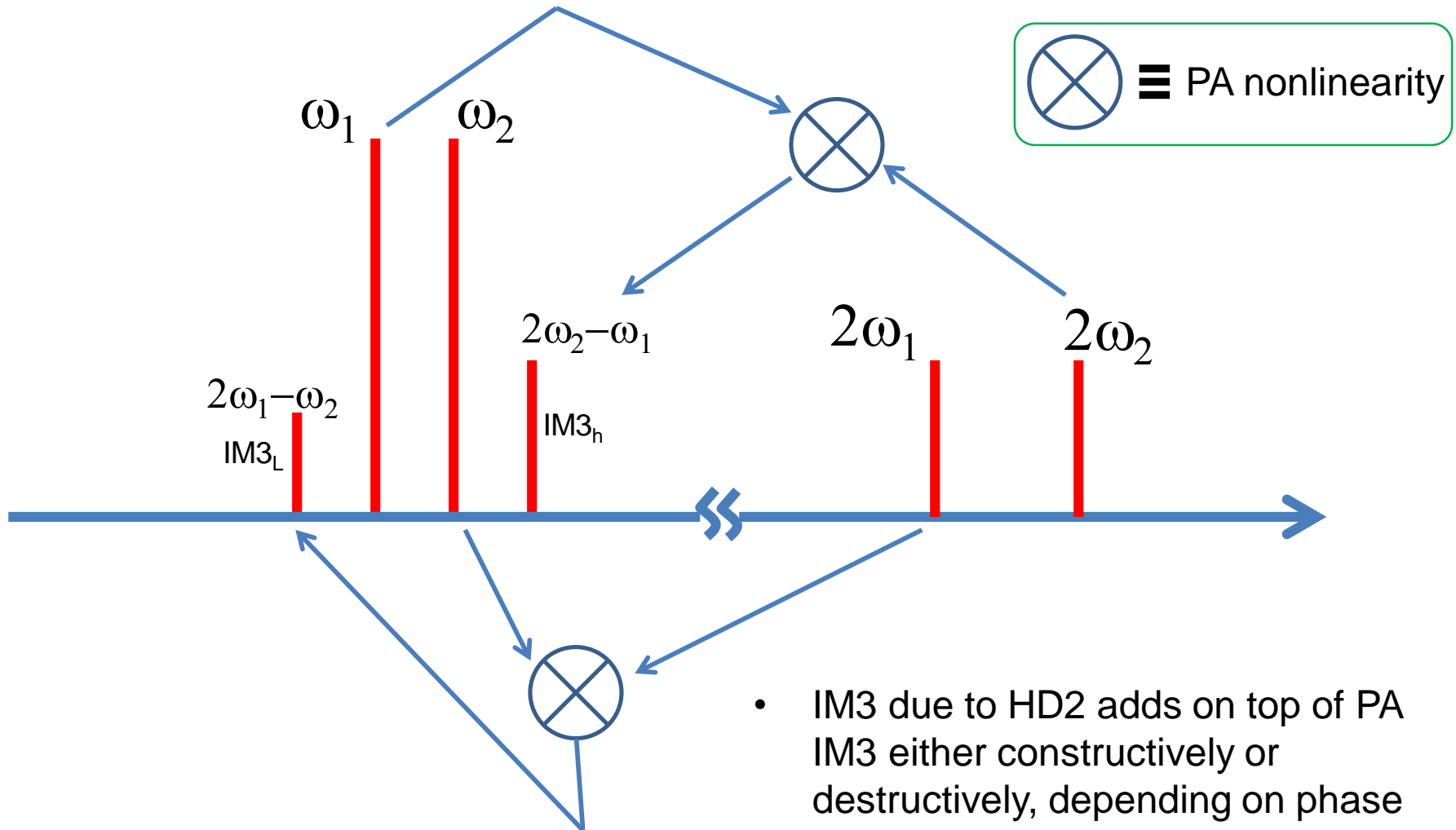
• terminating second order harmonics helps mitigate this mixing effect but impedance should be low and flat (resistive) over BW

Memory effects: IM3 asymmetry due to envelop

ω_1 ω_2

$\bigotimes$ ≡ PA nonlinearity

$\omega_2-\omega_1$

$2\omega_2-\omega_1$

$2\omega_1-\omega_2$

IM3$_L$

IM3$_h$

• Linearizing PA helps reduce the transfer function by which memory effects gets inband
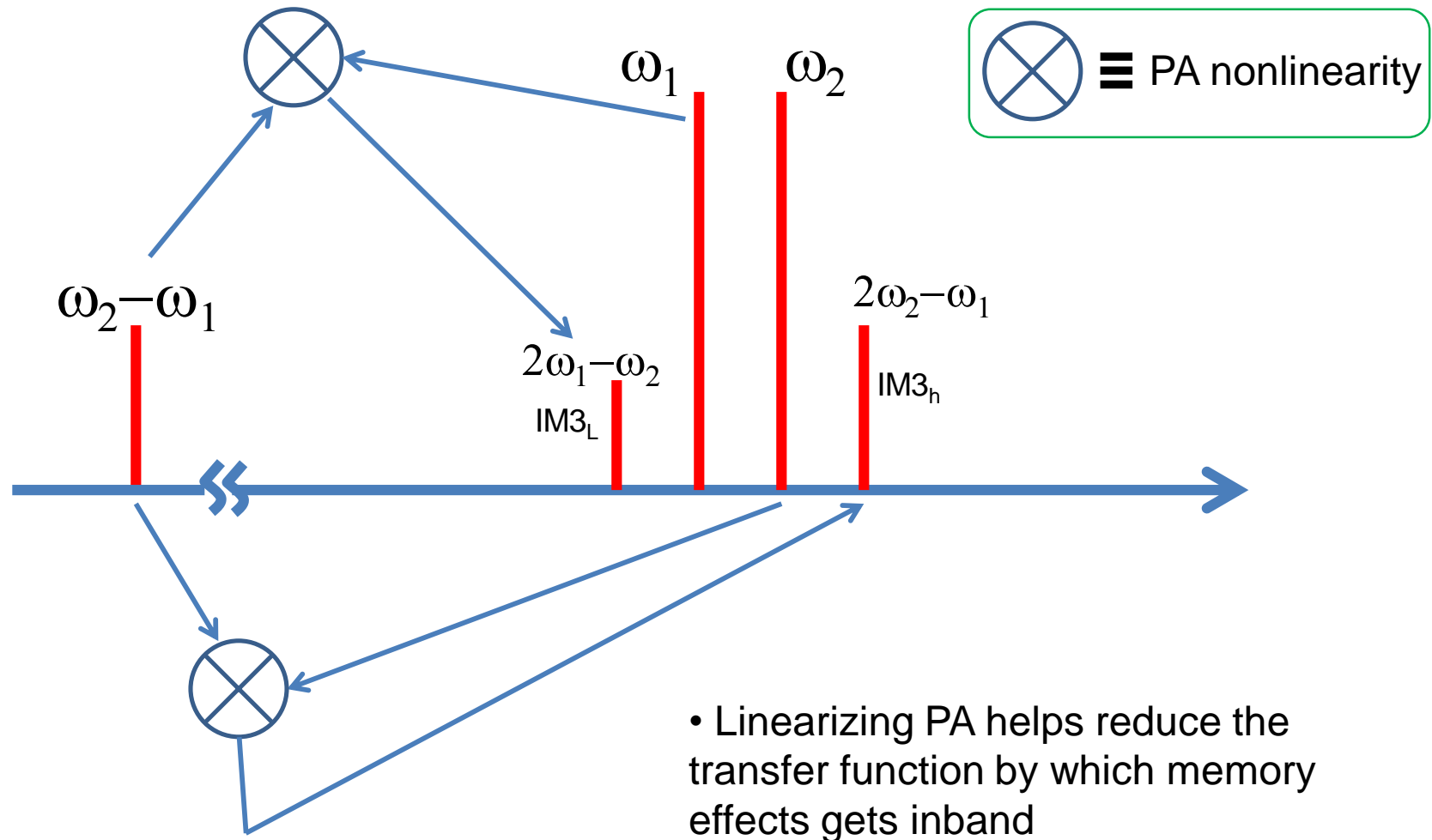
• designing bias circuits with low resistive output impedance and high BW compared to signal envelope helps mitigate this mixing effect difference to upper/lower sides

Memory effects: IM3 asymmetry due to envelop

Let us represent the two tone currents as:

$$i_1 = \cos(\omega_1 t) \quad ; \quad i_2 = \cos(\omega_2 t)$$

The low-frequency current component due to second order distortion can be calculated as:

$$\alpha_2 (i_1 + i_2)^2 = \frac{\alpha_2}{2} \cos(\Delta\omega t) \, ; \text{where } \Delta\omega = \omega_2 - \omega_1$$

If the impedance at $\Delta\omega$ has an imaginary part, it can be represented as $|Z|e^{j\theta}$

Therefore, the voltage at such node is I x Z, and so can be represented as:

$$v_{IM2} = \alpha_2 \frac{|Z|}{2} \cos(\Delta\omega t + \theta)$$

When v_{IM2} mixes with the two tones at that node due to 3rd order nonelinearity, it results in:

$$IM3_L = \alpha_3 [v_{IM2} \times \cos(\omega_1 t)] = \alpha_2 \alpha_3 \frac{|Z|}{4} \cos[(2\omega_1 - \omega_2 t) - \theta]$$

$$IM3_H = \alpha_3 [v_{IM2} \times \cos(\omega_2 t)] = \alpha_2 \alpha_3 \frac{|Z|}{4} \cos[(2\omega_2 - \omega_1 t) + \theta]$$

• It can be seen that the phase of the termination impedance, θ, at $\Delta\omega$ due to its imaginary part causes the $IM3_L$ and $IM3_H$ to be different and so one adds constructively and the other destructively to the PA's own IM3

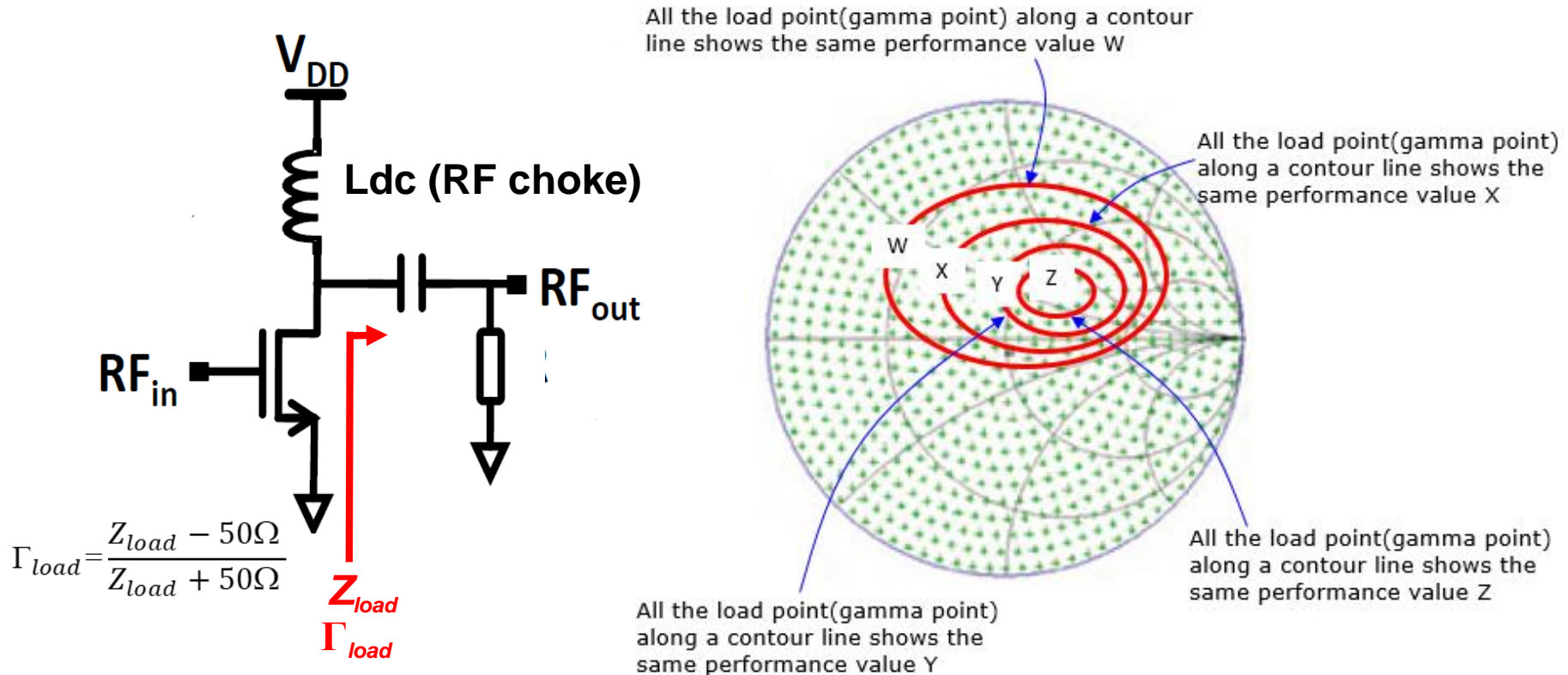# Memory effects: IM3 asymmetry due to envelop, cont

From previous slide it was found out that:

$$IM3_L = \alpha_3 [v_{IM2} \times \cos(\omega_1 t)] = \alpha_2 \alpha_3 \frac{|Z|}{4} \cos[(2\omega_1 - \omega_2 t) - \theta]$$

$$IM3_H = \alpha_3 [v_{IM2} \times \cos(\omega_2 t)] = \alpha_2 \alpha_3 \frac{|Z|}{4} \cos[(2\omega_2 - \omega_1 t) + \theta]$$

• Therefore, in order to reduce memory effects and asymmetry between
$IM3_L$ and $IM3_H$ as a function of $\Delta\omega$, you need to do the following:
1.   Reduce θ to zero (termination impedance at envelop frequency $\Delta\omega$ be
     real or resistive, no imaginary part)
2.   If θ cannot be reduced to zero, you can reduce termination impedance
     at envelope frequency |Z| to a very small value (for example use
     inductor to bias the PA which provides low impedance at envelop
     frequencies)
3.   Reduce the transfer function (PA nonelinearity at each node)
     parameters $\alpha_2 \alpha_3$ by which memory effects makes it to RF.

Choosing the optimum PA load: load-pull

V$_{DD}$

Ldc (RF choke)

RF$_{out}$

RF$_{in}$

$$\Gamma_{load} = \frac{Z_{load} - 50\Omega}{Z_{load} + 50\Omega}$$

Z$_{load}$

Γ$_{load}$

All the load point(gamma point) along a contour line shows the same performance value W

All the load point(gamma point) along a contour line shows the same performance value X

W X Y Z

All the load point(gamma point) along a contour line shows the same performance value Z

All the load point(gamma point) along a contour line shows the same performance value Y

• load-pull is sweeping PA drain load impedance (green dots on Smith Chart above) and plot contours of same performance parameters
• w, x, y z above can be Pout, PAE, gain, AM-AM/PM, V$_{swing}$, etc
• multi-dimensional sweep adds Vgs dc bias sweep, device size sweep, Rs sweep, etc.
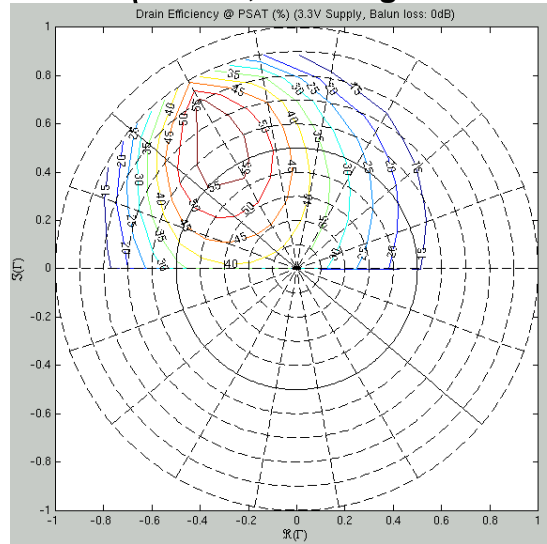→ Select the optimum load that meets all requirements Copyright© Dr. Osama Shana'a

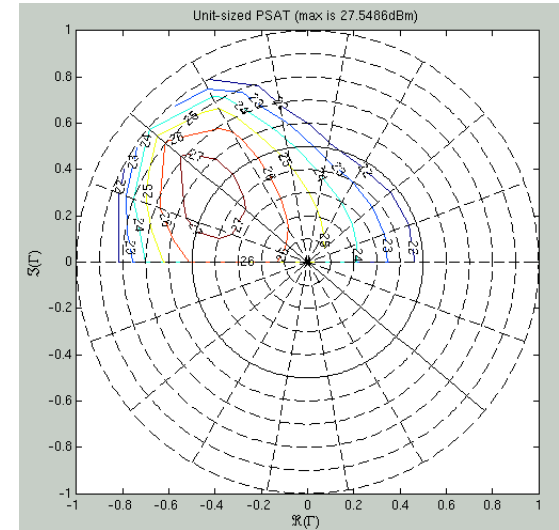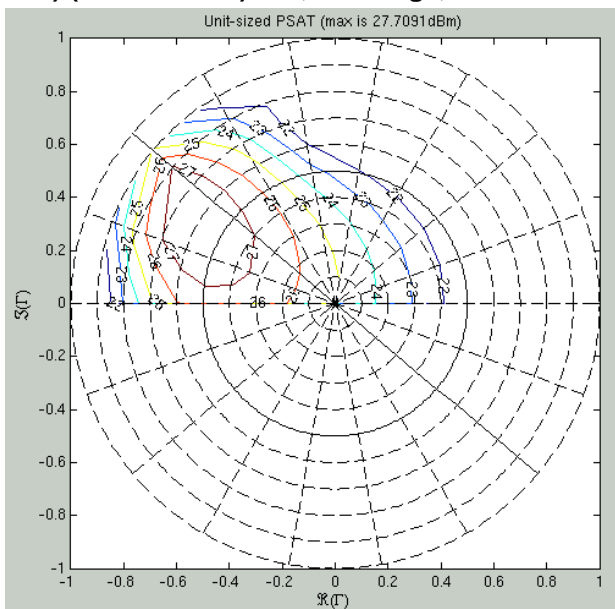# Load pull: how it looks like, example

Vswing @Psat, 0.55V Vgs
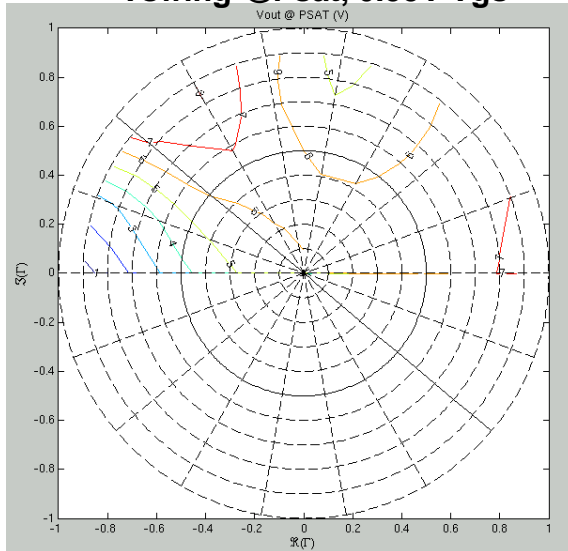
η @Psat, 0.55V Vgs

Psat, 0.55V Vgs

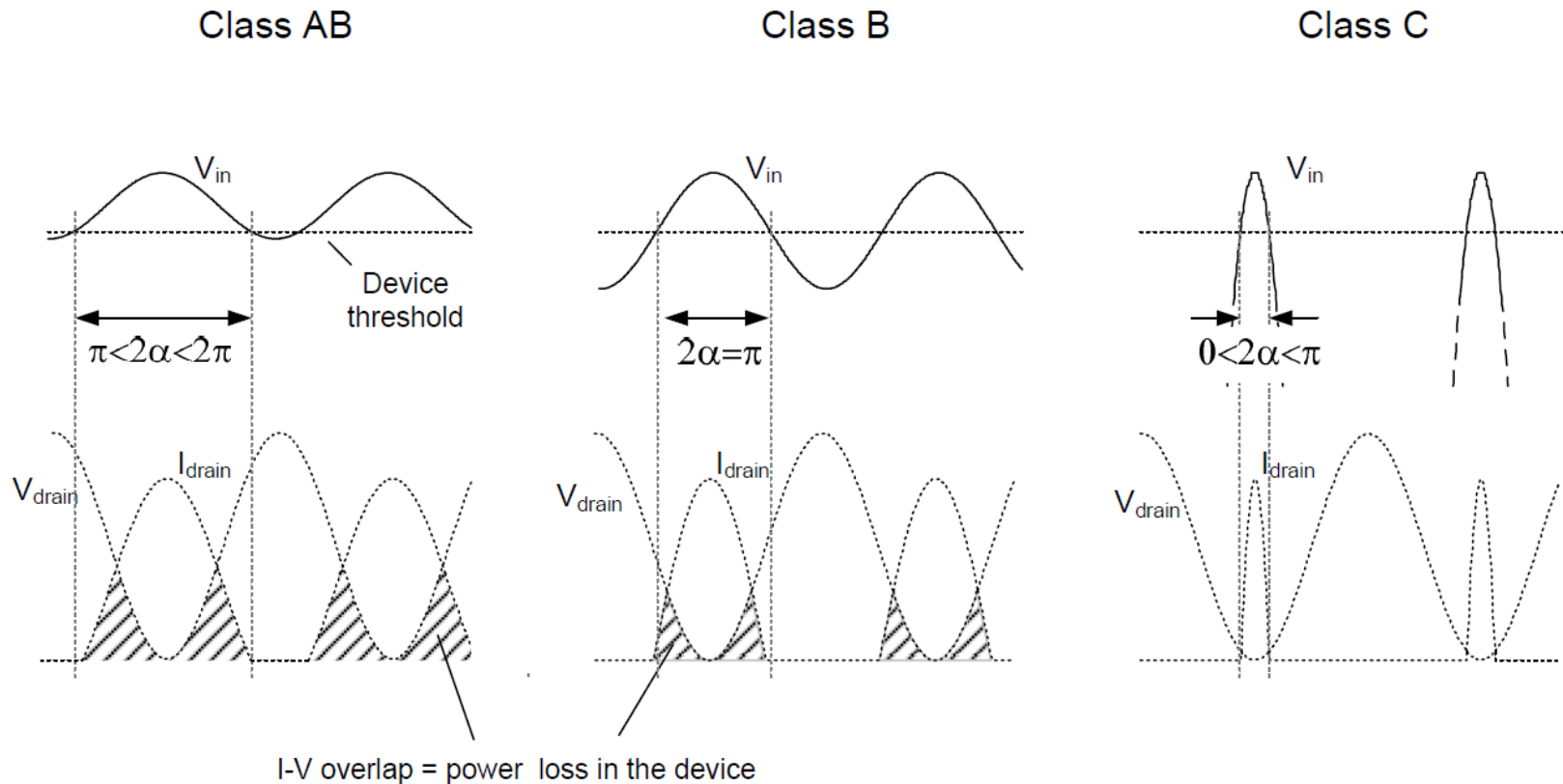**(Wio/Lio)/(Wcore/Lcore)=1/2, 0.55V Vgs, max Psat 27.7dBm**

• a simulator like Spectre or ADS is used to sweep circuit parameters (Vgs bias, device size, Pin, etc) and plot contours of Pout, efficiency, output swing, Psat, AM-AM/PM etc.

• matlab script is used to discard load impedances that do not meet PA specs (for example swing exceeds reliability, efficiency is too low, Psat is too low, etc.

• optimum impedance is then selected

PA DC bias sets its class: Class A, B, AB, C
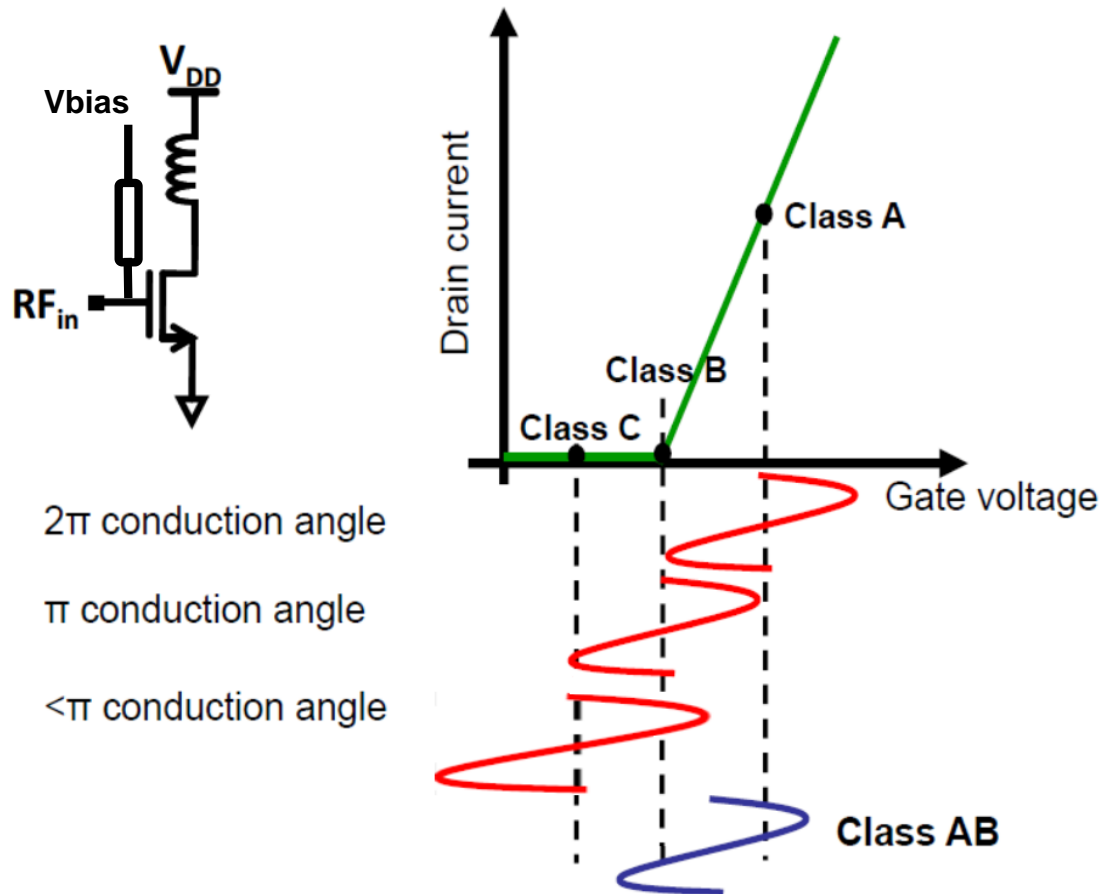
• Vbias sets the class of PA.
• class A is most linear but least efficient. Class C is most efficient of the 4 modes above but most none-linear

PA DC bias sets its class: Class A, B, AB, C

Class AB — $\pi < 2\alpha < 2\pi$, Device threshold

Class B — $2\alpha = \pi$

Class C — $0 < 2\alpha < \pi$

I-V overlap = power loss in the device

• more overlap between device voltage and current results in lower efficiency
• more efficient PA (class C) is generally more nonelinear and provides lower gain
• power dissipated into the device generates heat (thermal)
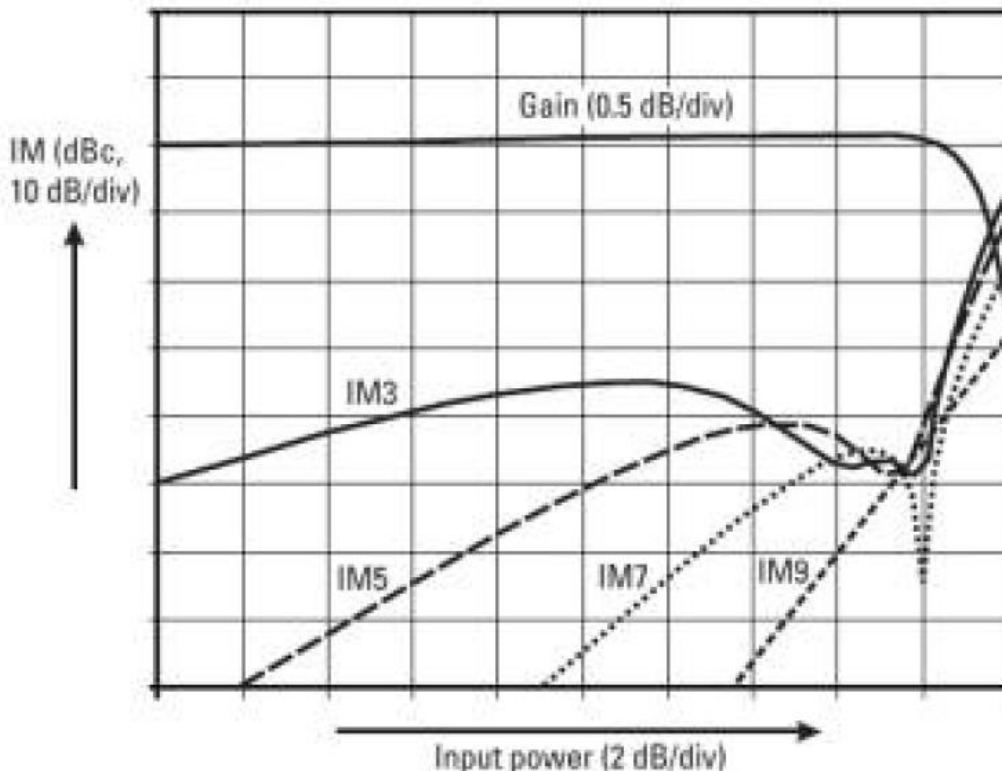
PA DC bias sets its class: Class E, F

Class-E amplifier   Class-E Voltage and Current waveforms

Class-F amplifier   Class-F Voltage and Current waveforms
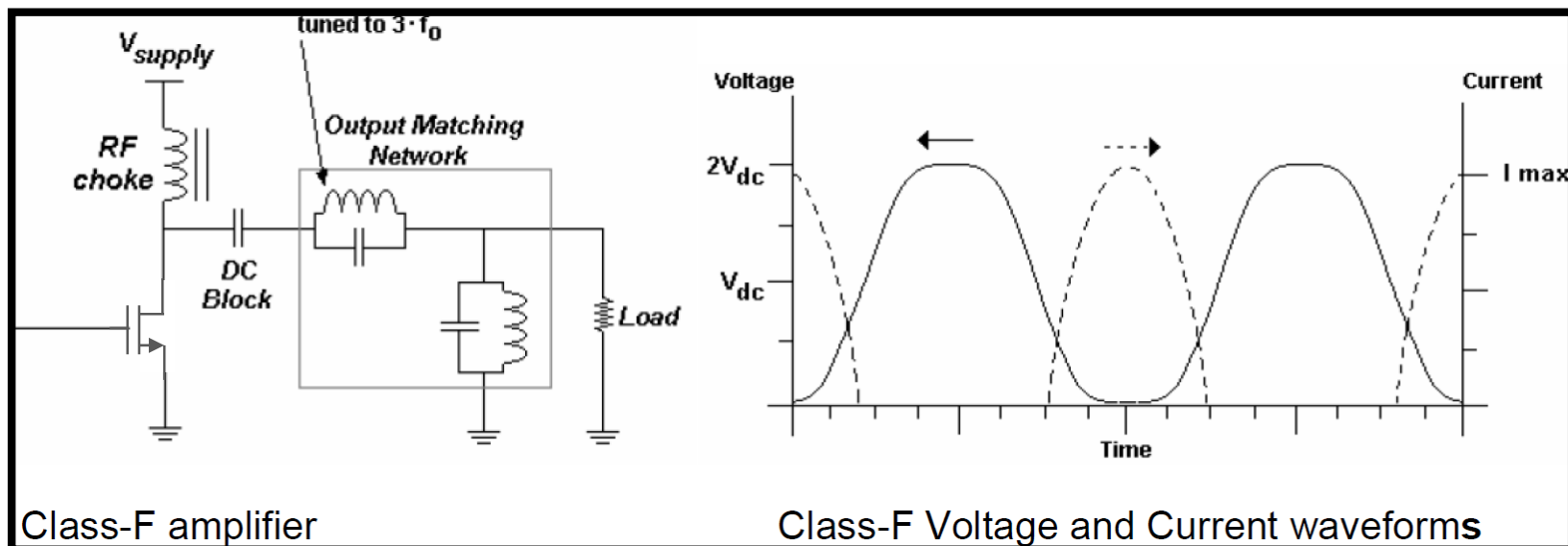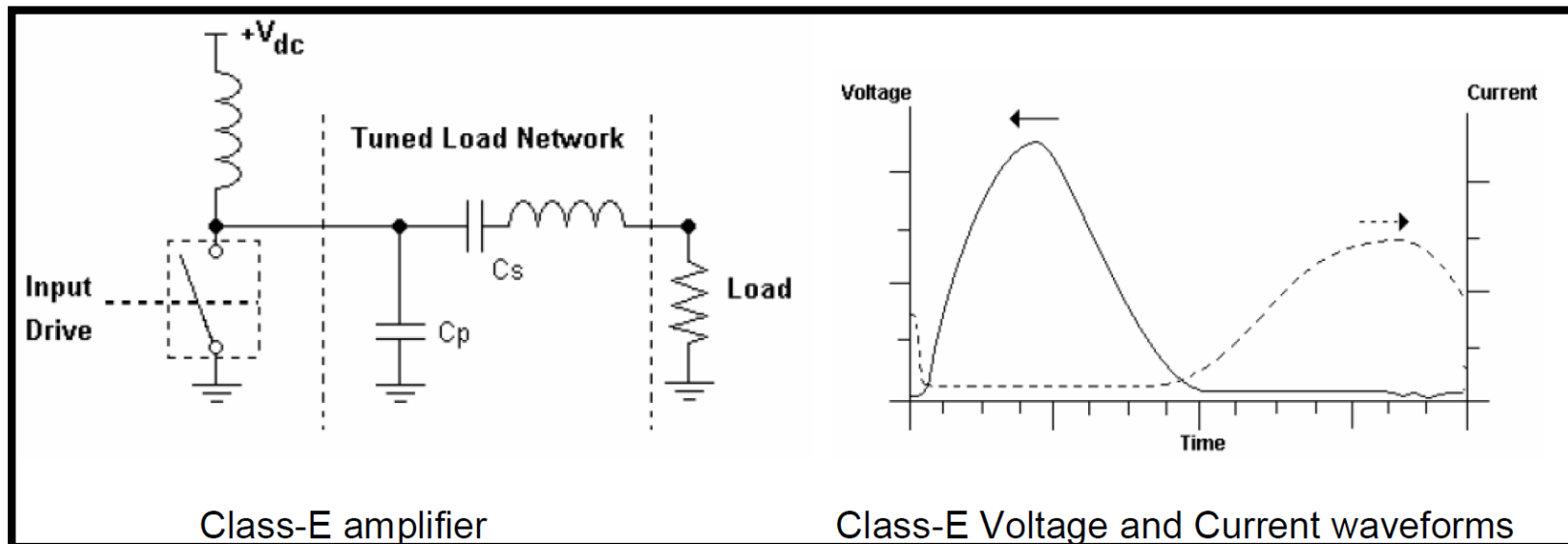
PA In-band distortion: IM3, IM5, IM7 interaction

$two - tones$: $S1$ at $f1$, $S2$ at $f2$

$3rd$ $oder$ $distorion$: $2f1 - f2$, $2f2 - f1$

$5th$ $oder$ $distorion$: $(3f1 - 2f2)$, $(3f2 - 2f1)$, $(2f1 - f2)$, $(2f2 - f1)$

$7th$ $oder$ $distorion$: $(4f1 - 3f2)$, $(4f2 - 3f1)$, $(3f1 - 2f2)$, $(3f2 - 2f1)$,
$(2f1 - f2)$, $(2f2 - f1)$


• at small Pin/Pout, IM(n) has a slope of (n) vs Pin
• at large Pin/Pout, 3rd and 5th (7th, etc.) order distortion generate distortion components at exact same frequencies but with different phases. In some cases, the phase may result in partial cancellation which shows improvement in IM3 at high Pout for some PAs.

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Two-stage PA:

driver-stage   Inter-stage matching balun   Power-stage
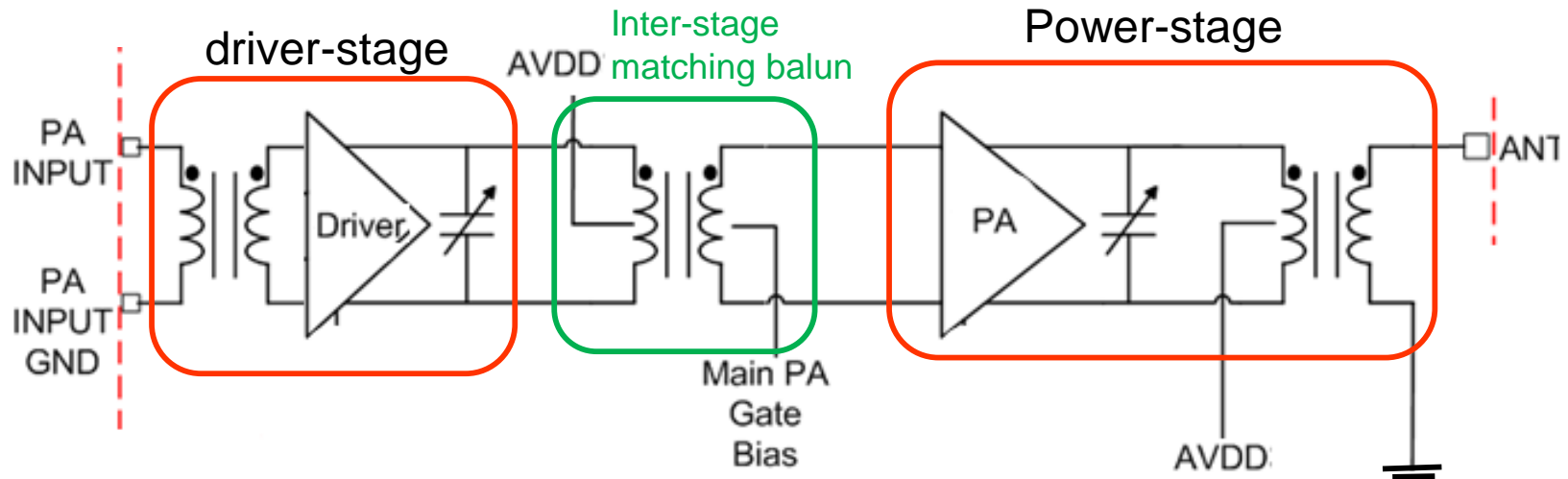
- The PA stage (called sometimes the power stage) delivering power to the load may not have sufficient power gain (especially if it is class C or class AB)

- as a result, a PA-driver stage is added to boost the overall PA gain

- a matching network (usually balun) is used to boost the low input impedance of the large PA power stage seen by the PA driver stage

- the overall PA efficiency must include the PA-driver stage.

- a typical PA power gain is 25~30dB.

- driver stage is usually made to be very linear (class-A) to prevent higher-order distortion inside PA of signals coming from this stage

Efficiency degradation due to PAPR:
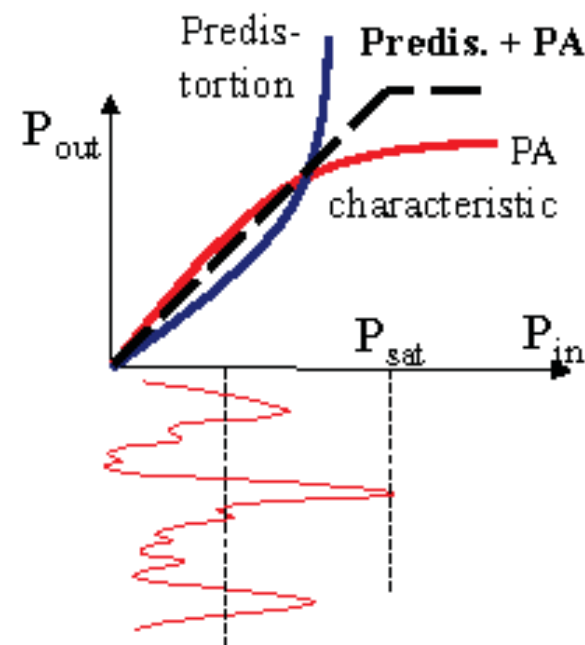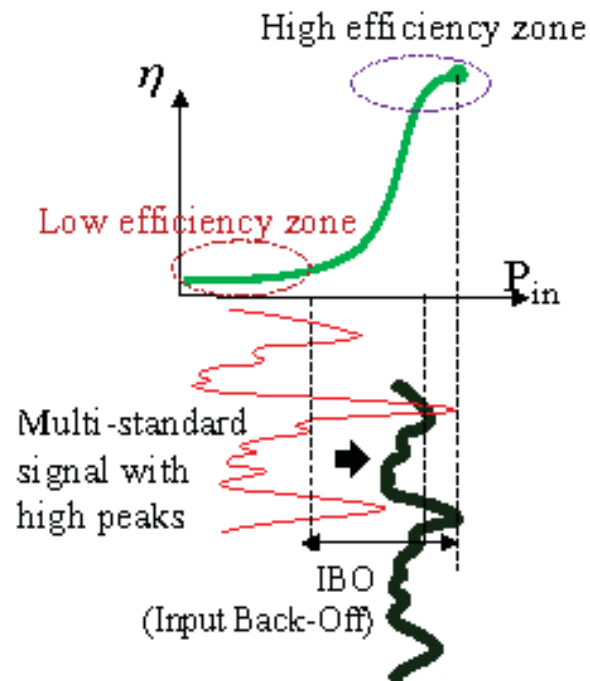
• as we discussed in previous lectures, PA efficiency degrades quite rapidly vs backoff power from Psat
• it will be "nice" to see if PA does not need to backoff and still support large PAPR → how?

# Efficiency enhancer: PAPR (crest factor) reduction
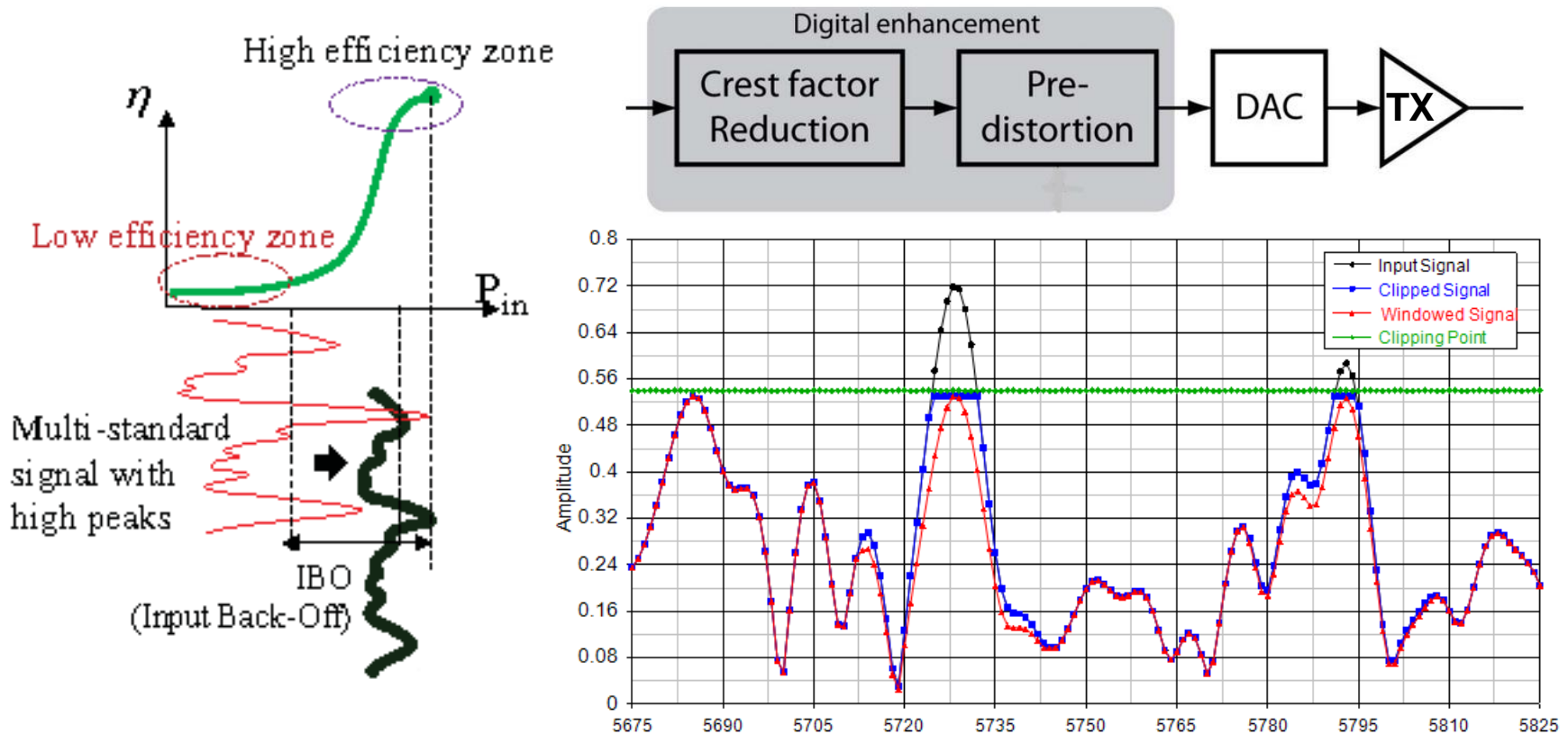
- if PAPR is reduced, less backoff is needed → efficiency is improved
- PAPR reduction degrades in-band EVM. Therefore, for it to work, the receiver needs to apply the inverse reduction function to recover signal back. Not all standards support this → do PAPR reduction only for relaxed EVM modulations, for example MCS0 in WiFi.

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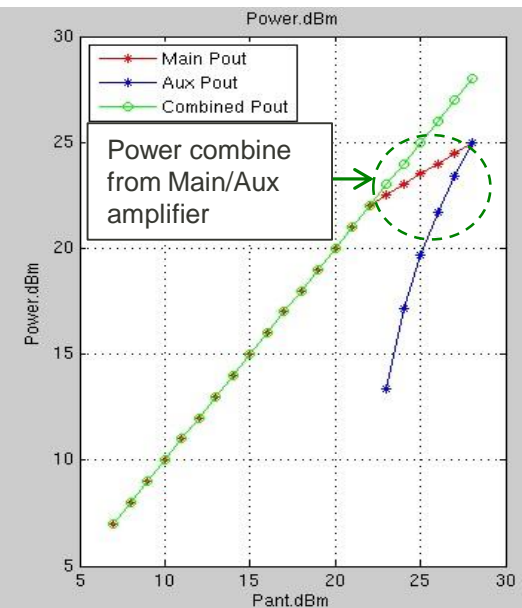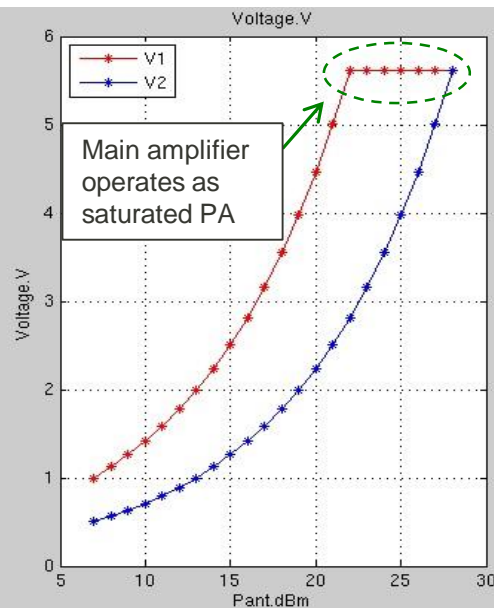# Efficiency enhancer: active load modulation, Doherty PA
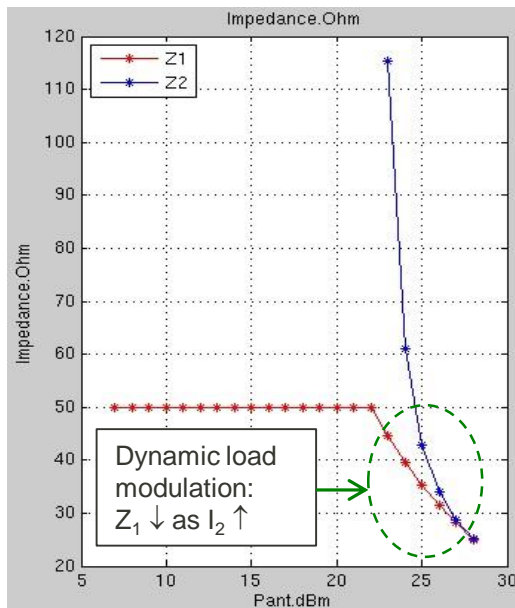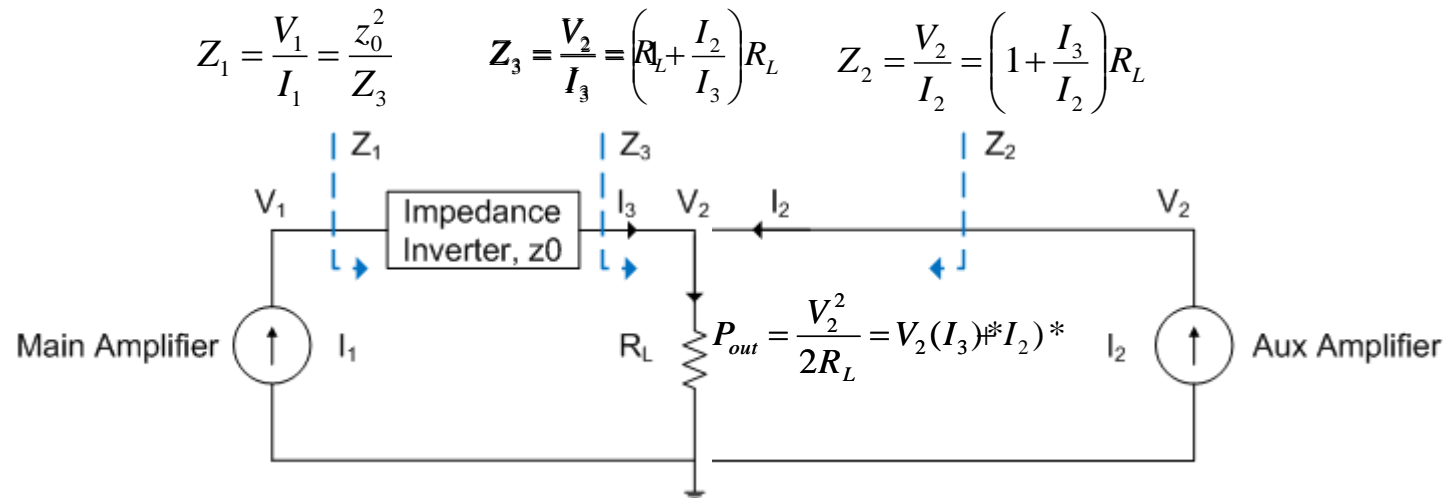

Impedance Inverter/transformer
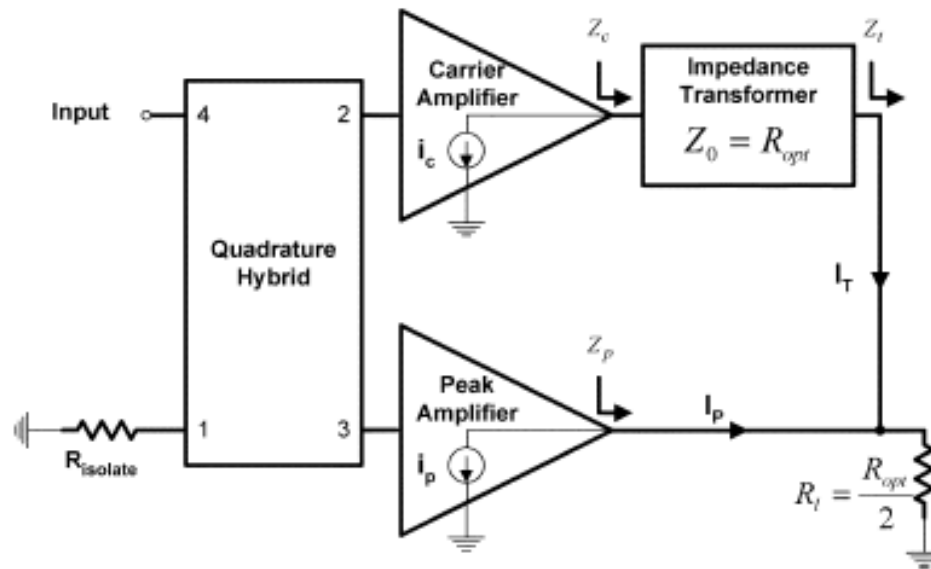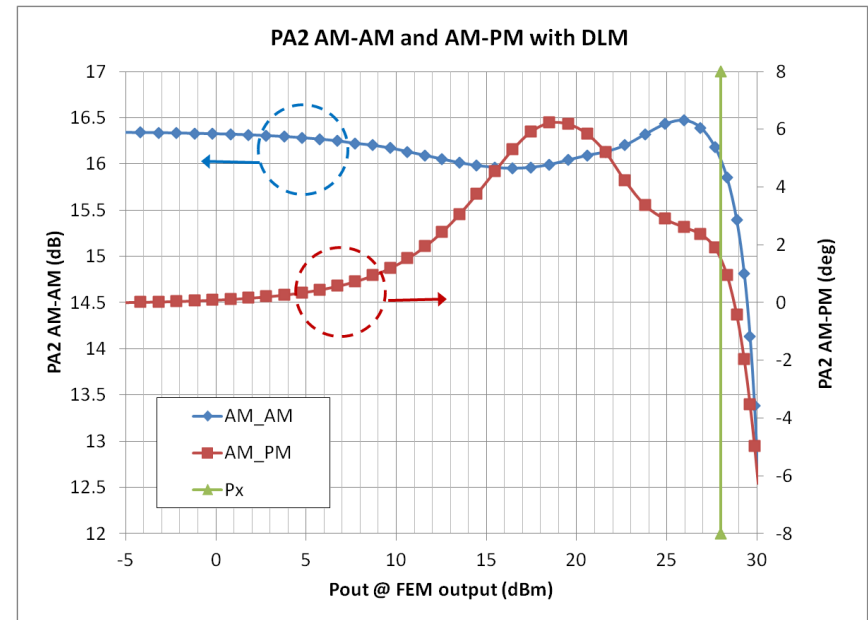
Zc reduces as Ip increase
→ active load modulation.
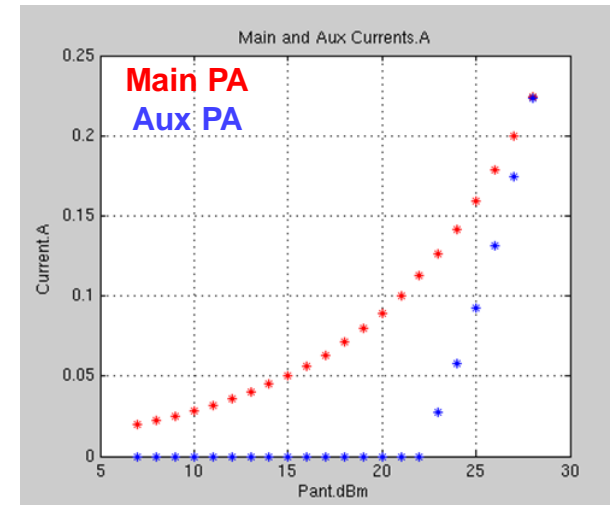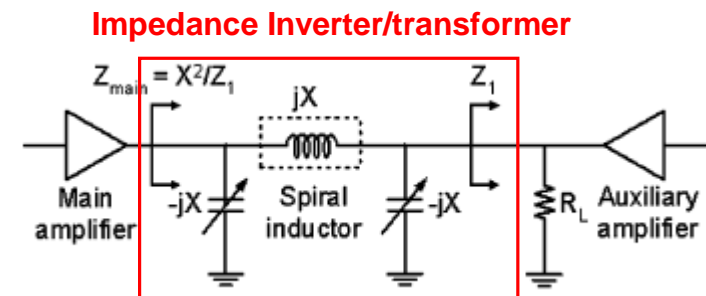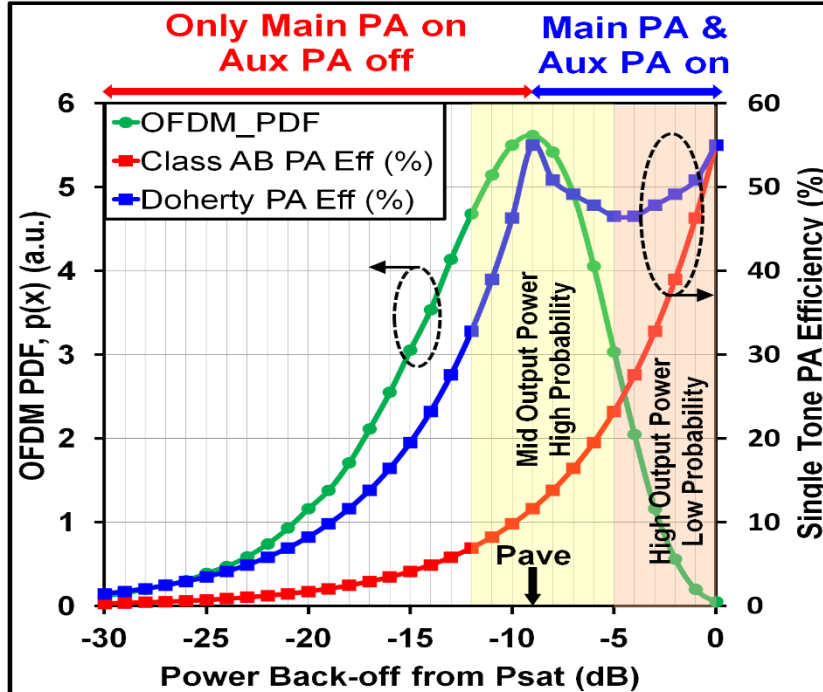
• Doherty PA has two power amplifiers; Main to deliver average power and Aux to deliver peak power. They are biased at different points. Aux PA starts to turn-on once Pout crosses the average power level

• impedance inverter results in dynamic load modulation. As a result, two peaks show up in efficiency plot

• problem with Doherty PA is its nonlinearity, especially strong memory effects

Concept of Doherty PA:

$$Z_1 = \frac{V_1}{I_1} = \frac{z_0^2}{Z_3} \qquad Z_3 = \frac{V_2}{I_3} = \left(R_L + \frac{I_2}{I_3}\right)R_L \qquad Z_2 = \frac{V_2}{I_2} = \left(1 + \frac{I_3}{I_2}\right)R_L$$


$$P_{out} = \frac{V_2^2}{2R_L} = V_2(I_3)*I_2)*$$

Efficiency enhancement: Doherty PA

- for low Power, only Main PA is on (half size of class AB). When Power reaches Pave (PAPR below Psat), Main PA reaches Psat-3dB and Aux PA turns on and so efficiency reaches its first peak. As Pout increases, Aux turns on more and efficiency reaches its second peak at Psat.
- Doherty improves efficiency over class AB PA almost by 2x for output stage (if you ignore driver)
- As seen from AM-AM/PM, Doherty has severe distortion and so DPD is a must (memory DPD most of the time)

Example Doherty PA: WiFi 11ac Front-end Module (FEM)

[1] Chee, et, al. ISSCC 2017
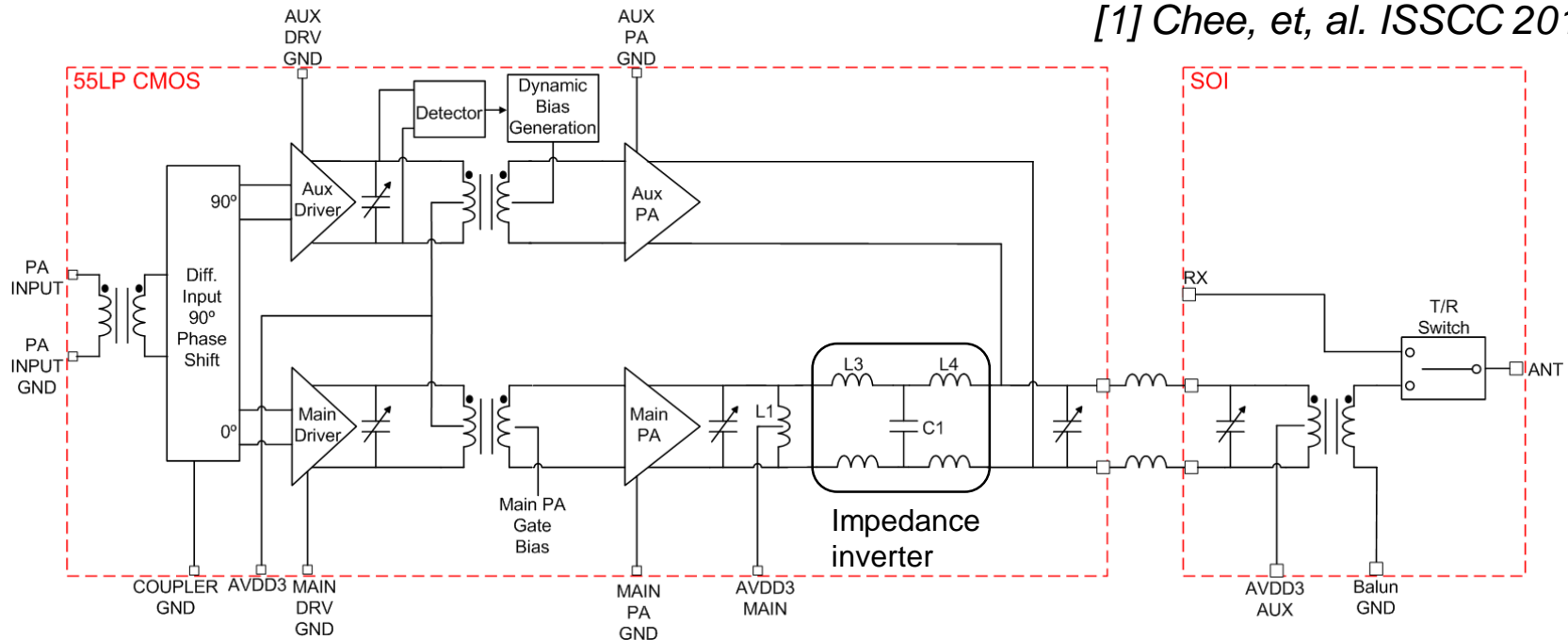
- two stage impedance inverter for 1GHz RF bandwidth (WiFi 6GHz 11ac/ax)
- input coupler/power-splitter causes a 90-degree phase shift. Impedance inverter also causes 90-degree phase shift, so both Main and Aux currents are combined in-phase
- when Main and Aux PAs are of same size, the PA is called "symmetric Doherty PA". At Psat, Main and Aux deliver equal power to the load. If Aux is to deliver most of the PAPR power, Aux PA size has to be larger than Main PA (asymmetric design)

Efficiency enhancement: Envelop tracking (ET)

Vdd

3GPP power control slot time 0.5 ms / 1 ms
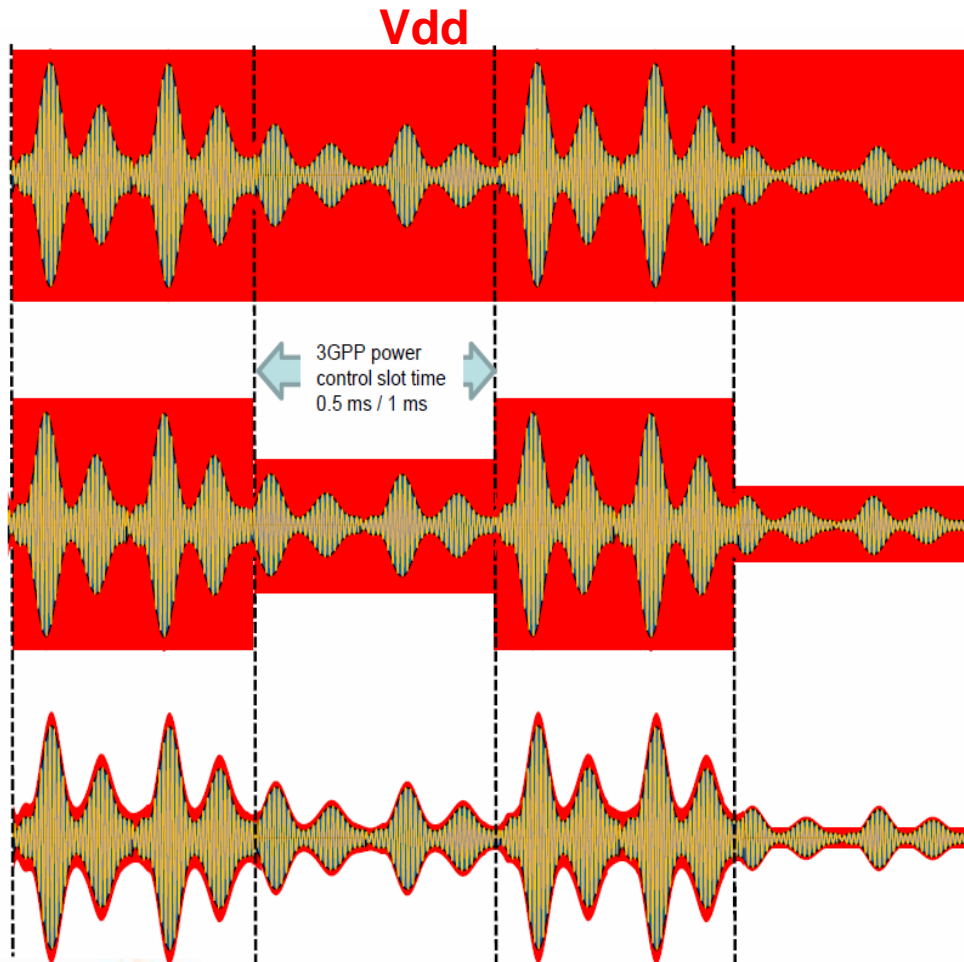
Wasted supply power

Fixed Supply
- Simple, but poor efficiency
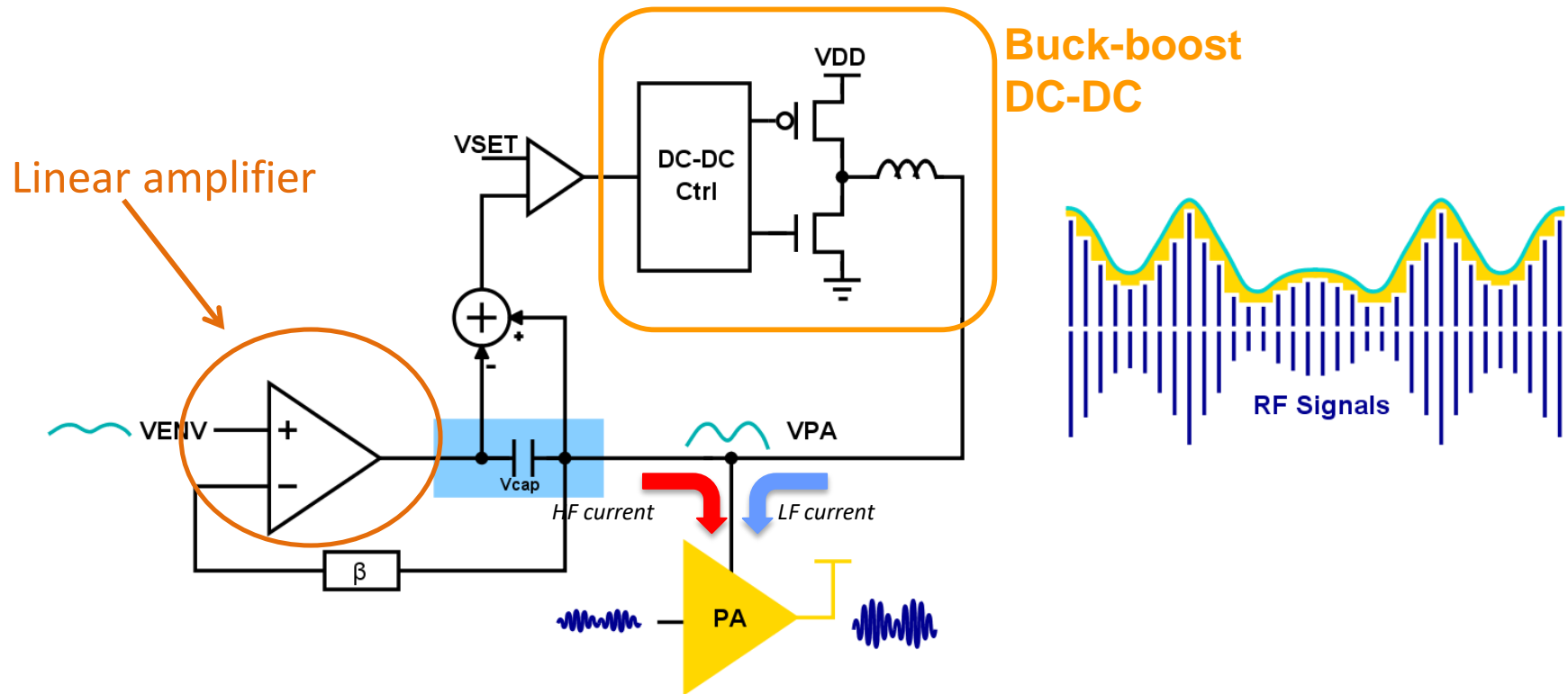- Efficiency is strong function of waveform PAPR.

Average Power Tracking (APT)
- Per-slot tracking based on TX power level
- Improves efficiency at low power.
- Doesn't help at high power.

Envelope Tracking (ET)
- Dynamic, high speed supply tracking of signal amplitude
- Improves efficiency
- Waveform-independent

Efficiency enhancement: continuous ET scheme

- ## LF path in parallel with HF path to track envelope.
  - LF path: high-efficiency to provide DC current (APT)
  - HF path: linear stage to provide AC current (ET)

Efficiency enhancement: continuous ET scheme
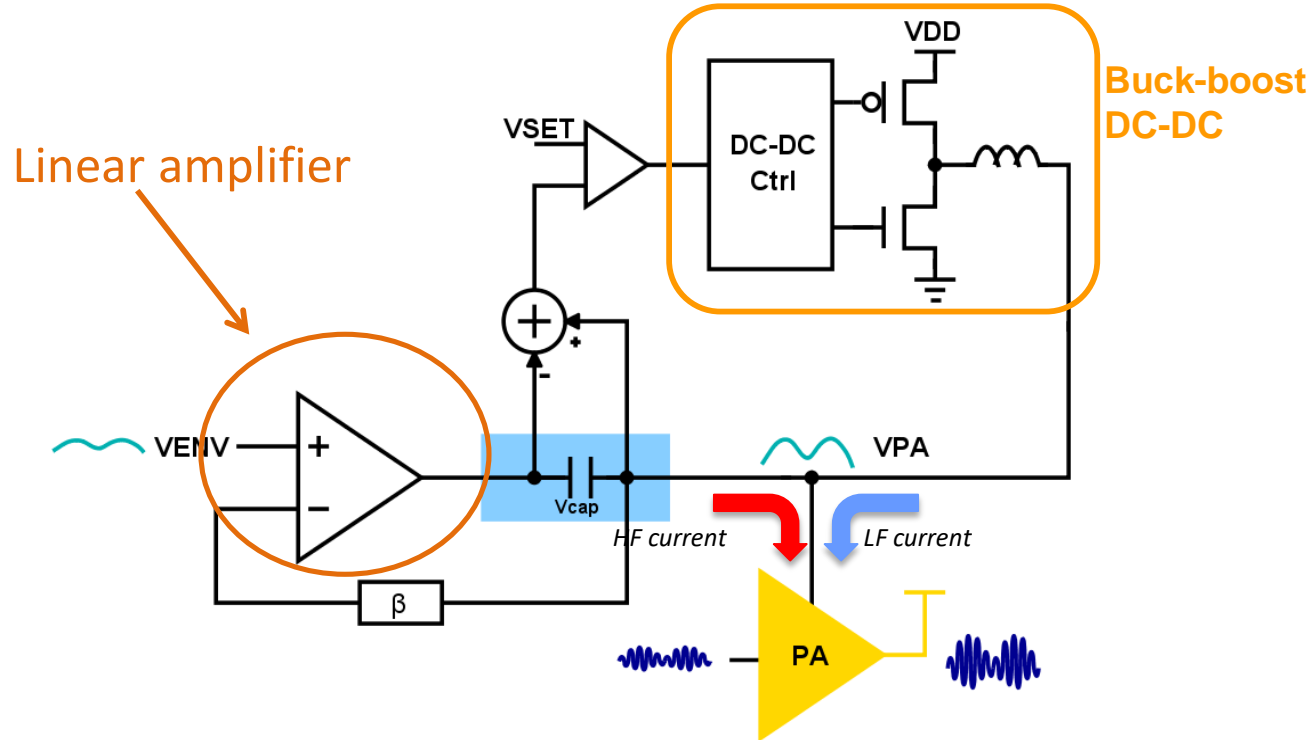
- amplifier distortion needs to be low over envelop (3~5x signal BW)→ needs current
- system efficiency drops fast as signal BW increases
- Requires stringent alignment between envelop signal (VPA) and input to PA (<1ns range) → extensive calibrations needed
- Does NOT work well for high BW (>200MHz) and low EVM systems (-33dBc)
- overhead is large and efficiency improvement is low for low PAPR systems (<5dB) like 3G cellular (overall system efficiency improvement is <5% to justify the cost)
- you need one of these for each PA (dual-band, MIMO, etc.)

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Efficiency enhancement: Discrete ET scheme
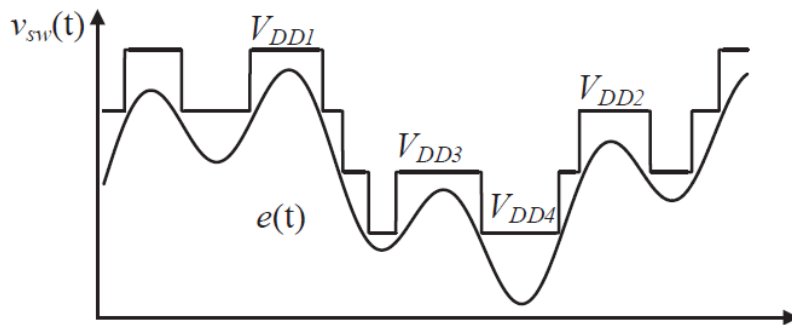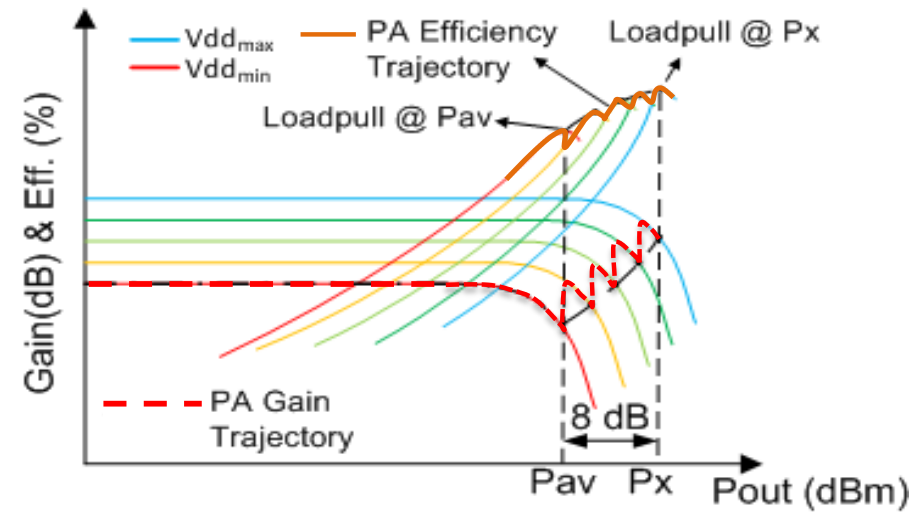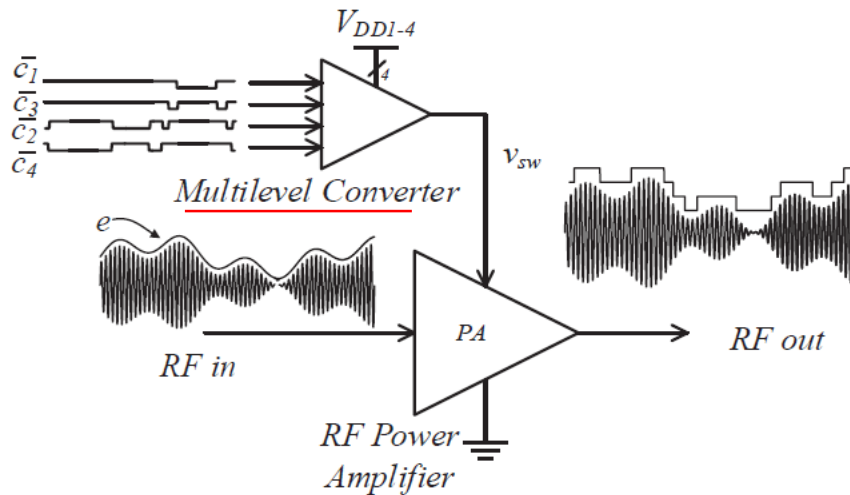
Limitation on Vdd:
- stress (upper)
-- knee (lower)

Other limitations include:
--Phase/gain over Vdd
-- memory effects

☺ • no high-speed linear amp needed

☺ • alignment requirement is relaxed

• needs good DPD

• modulator design is tricky

Alihossein Sepahvad, et al., ECCE 2016
Philip Godoy, et al., JSSC 2012

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[1] Yuen Hui Chee, Fatih Golcuk, Toru Matsuura, Christopher Beale, James F. Wang, and Osama Shanaa, "A Digitally Assisted CMOS WiFi 802.11ac/11ax Front-End Module Achieving 12% PA Efficiency at 20dBm Output Power with 160MHz 256QAM OFDM Signal," *ISSCC Dig. Tech. papers*, pp 292-293, Feb 2017

[2] C.P. Huang, et al., "A Highly Integrated Single Chip 5-6 GHz Front-end IC Based on SiGe BiCMOS that enhances 802.11ac WLAN Radio Front-End Designs", RFIC Dig. of Tech. Papers, pp. 227-230, May 2015

[3] Alihossein Sepahvand, Parisa Momenroodaki, Yuanzhe Zhang, Zoya Popovi´c, and Dragan Maksimovi´c, "Monolithic Multilevel GaN Converter for Envelope Tracking in RF Power Amplifiers," IEEE Energy Conversion Congress and Exposition, pp1-7, Sept 2016

[4] Philip A. Godoy, SungWon Chung, Taylor W. Barton, David J. Perreault, and Joel L. Dawson, "A 2.4-GHz, 27-dBm Asymmetric Multilevel Outphasing Power Amplifier in 65-nm CMOS," IEEE Journal of Solid-State Circuits, Vol. 47, No. 10, pp. 2372-2384, Oct. 2012

[5] Yehui Han and David J. Perreault, "Analysis and Design of High Efficiency Matching Networks," IEEE Transactions on Power Electronics, Vol. 21, No. 5, September 2006, pp. 1484-1491

[6] Domine Leenaerts, J. van der Tang, Cicero S. Vaucher, *Circuit Design for RF Transceivers*, Springer, 2007

[7] S.C. Cripps, *Advanced Techniques in RF power Amplifier De*sign, Norwood, Artech House, 2002

[8] Joel H. K. Vuolevi, et. al, "Measurement Technique for Characterizing Memory Effects in RF Power Amplifiers," IEEE TMTT, Vol. 49, No. 8, pp. 1383-1389, August 2001

[9] Joao Paulo Martins, et. al, "A Metric for the Quantification of Memory Effects in Power Amplifiers," IEEE TMTT, Vol. 54, No. 12, pp. 4432-4439, December 2006

[10] N. Wongkomet, L. Tee, and P. R. Gray, " A +31.5 dBm CMOS RF Doherty Power Amplifier for Wireless Communications", *IEEE JSSC*, vol. 41, pp. 2852-2859, Dec. 2006.